EE60032: Analog Signal Processing

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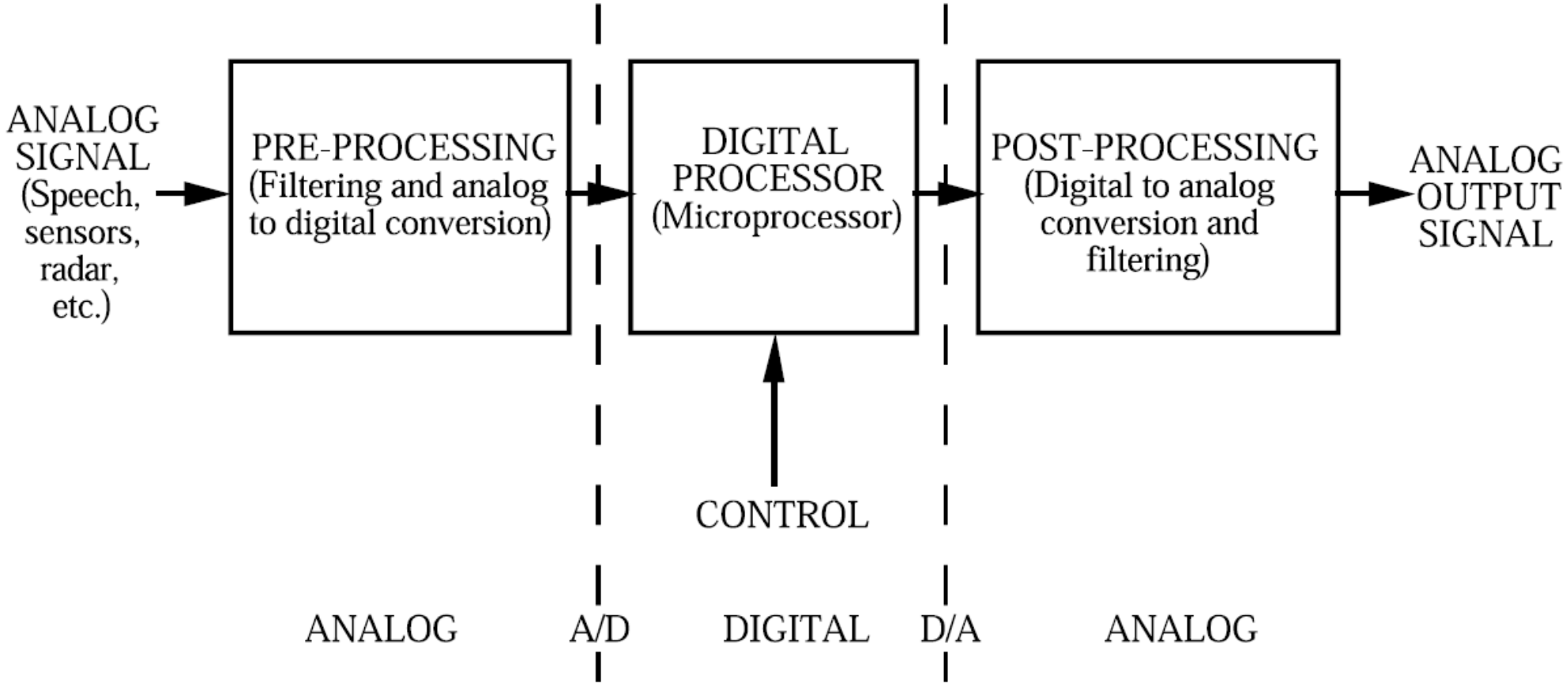
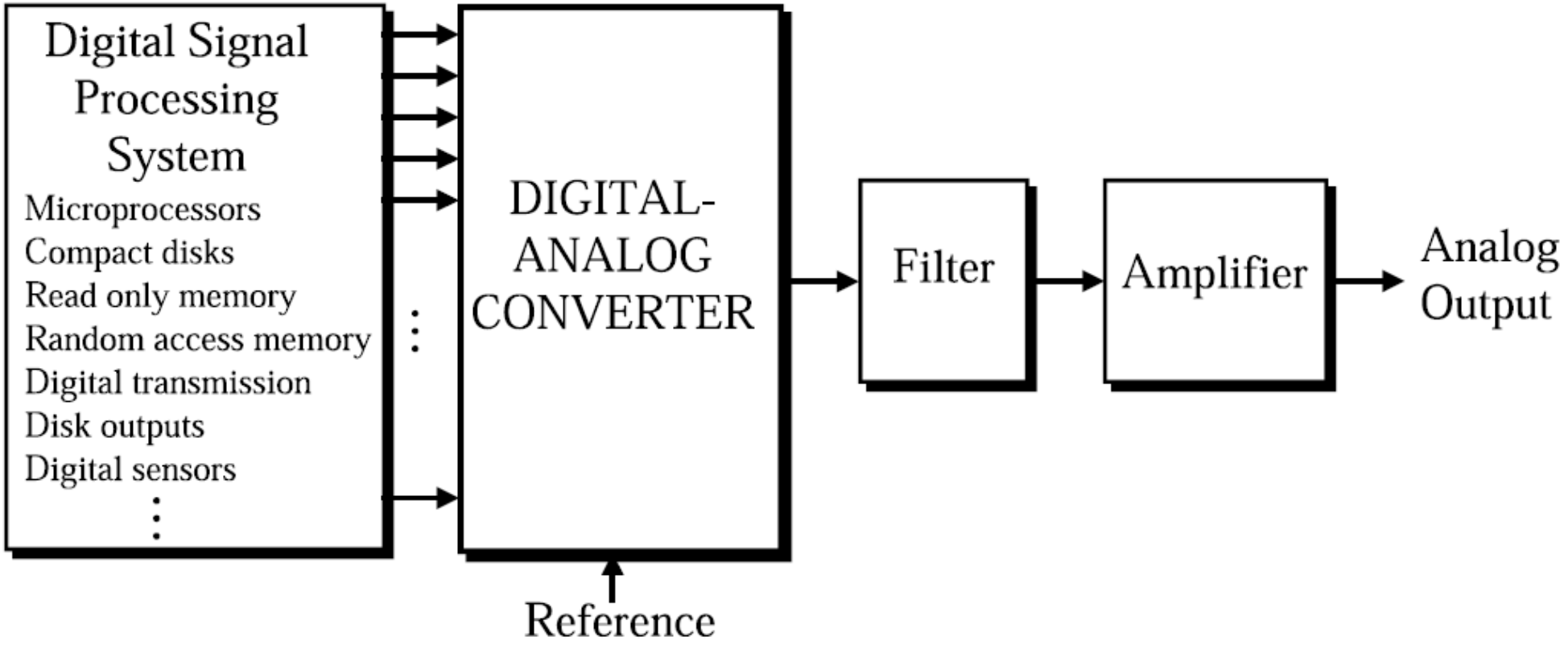
Module-3: Data Converters

Main Reference: CMOS Analog Circuit Design by Allen and Holberg, Oxford Indian Edition

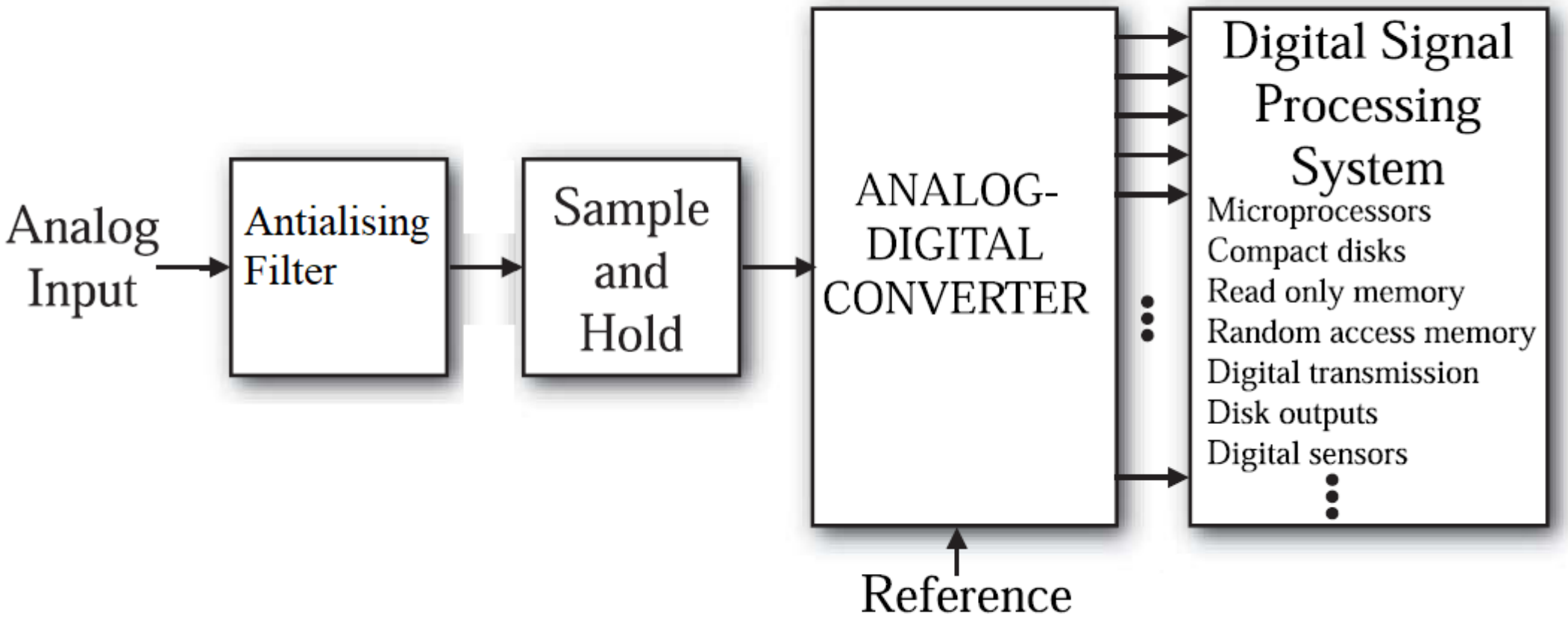
Importance of Data Converters in Signal Processing



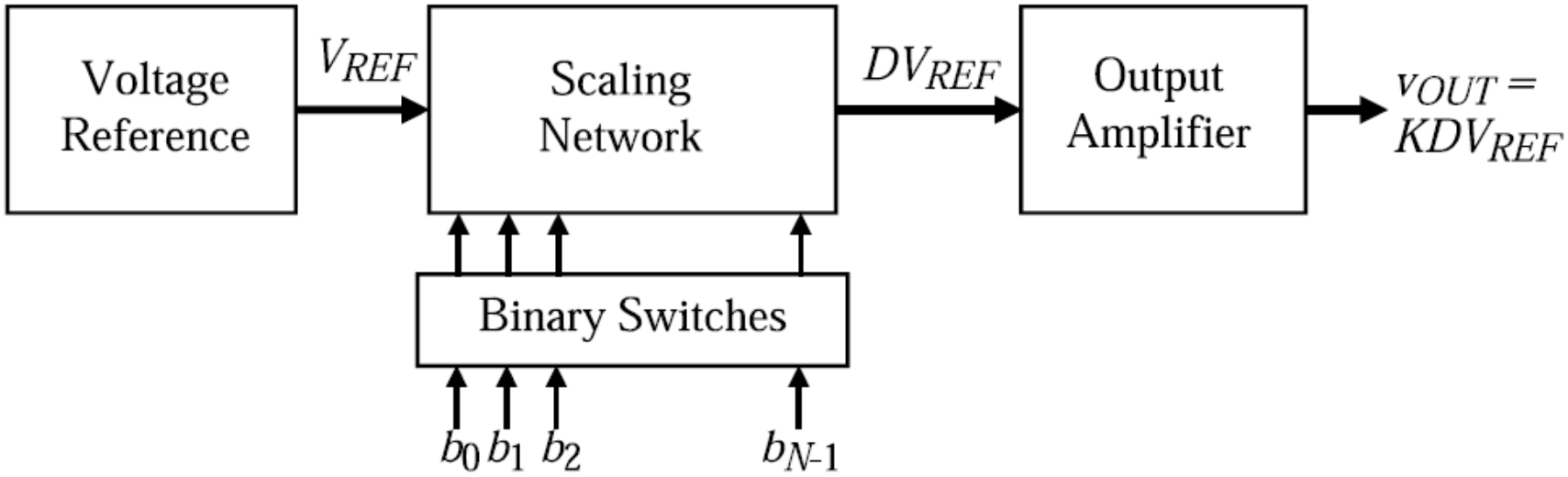
Digital-Analog Converters



Analog-Digital Converters



Block Diagram of a Digital-Analog Converter



b_0 is the most significant bit (MSB)

The MSB is the bit that has the most (largest) influence on the analog output

b_{N-1} is the least significant bit (LSB)

The LSB is the bit that has the least (smallest) influence on the analog output

Different performance characteristics of DAC:

- Static characteristics: Easy to estimate, important in low frequency operation
- Dynamic charactersistics: Difficult to estimate, important for medium and high frequency

Static Characteristics of Digital to Analog Converter

- Resolution: Equal to no. of bits
- The Full Scale (FS): (Analog output when all bits are one – Analog output when all bits are zero)

$$FS = \left(V_{REF} - \frac{V_{REF}}{2^N}\right) - 0 = V_{REF}\left(1 - \frac{1}{2^N}\right)$$

- Full Scale Range (FSR)

$$FSR = \lim_{N \to \infty}(FS) = V_{REF}$$

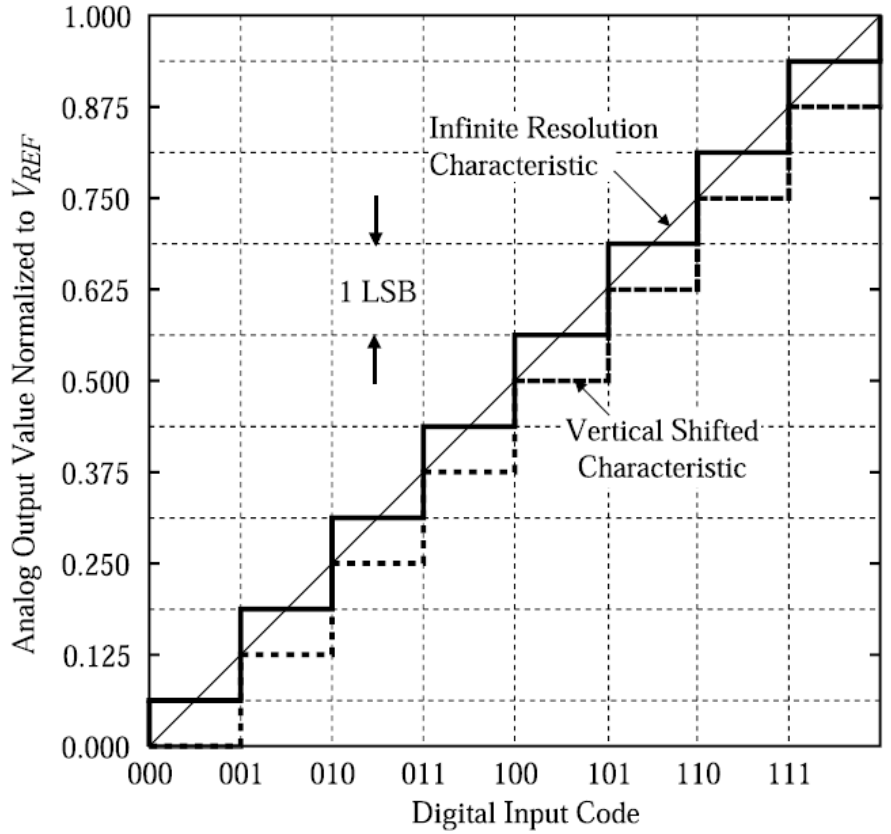
- Dynamic Range (DR): Ratio of FSR to the smallest difference that the DAC can resolved.

$$DR = \frac{FSR}{LSB\ \text{change}} = \frac{FSR}{(FSR/2^N)} = 2^N$$

or in terms of decibels

$$DR(\text{dB}) = 6.02N\ (\text{dB})$$

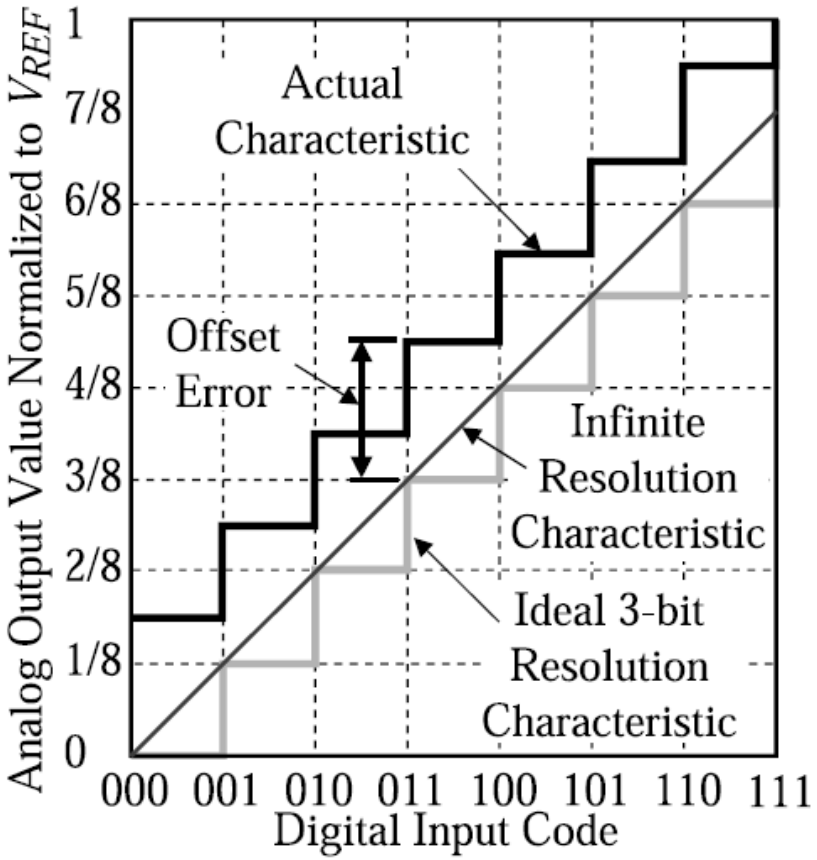
Ideal input-output characteristics of a 3-bit DAC



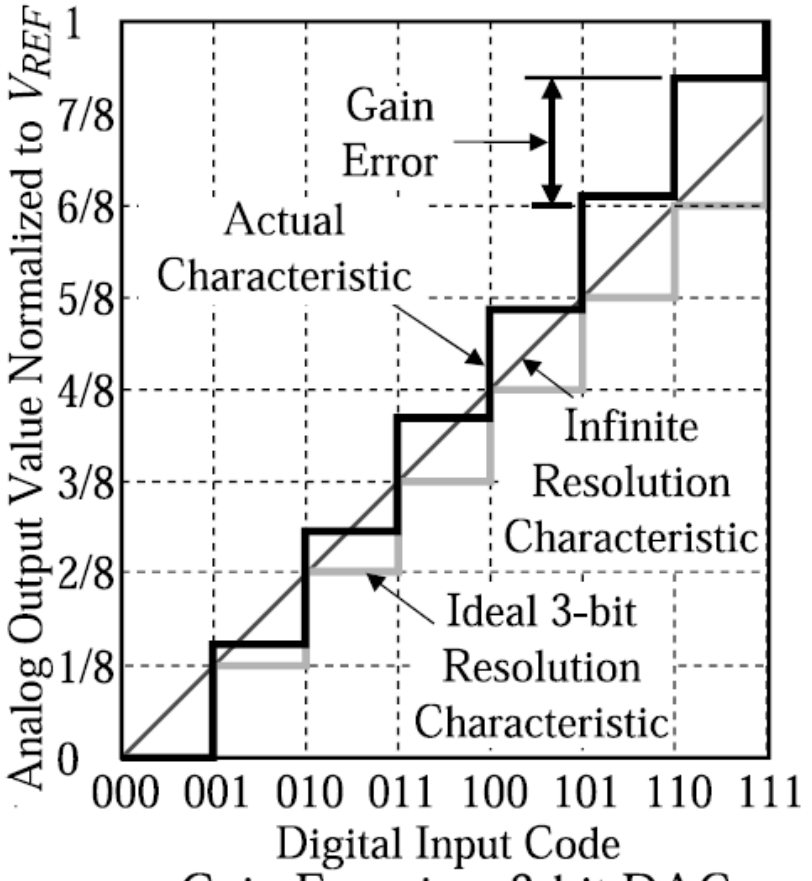
Offset and Gain Errors

An *offset error* is a constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at any vertical jump.

A *gain error* is the difference between the slope of the actual finite resolution and the ideal finite resolution characteristic measured at the right-most vertical jump.



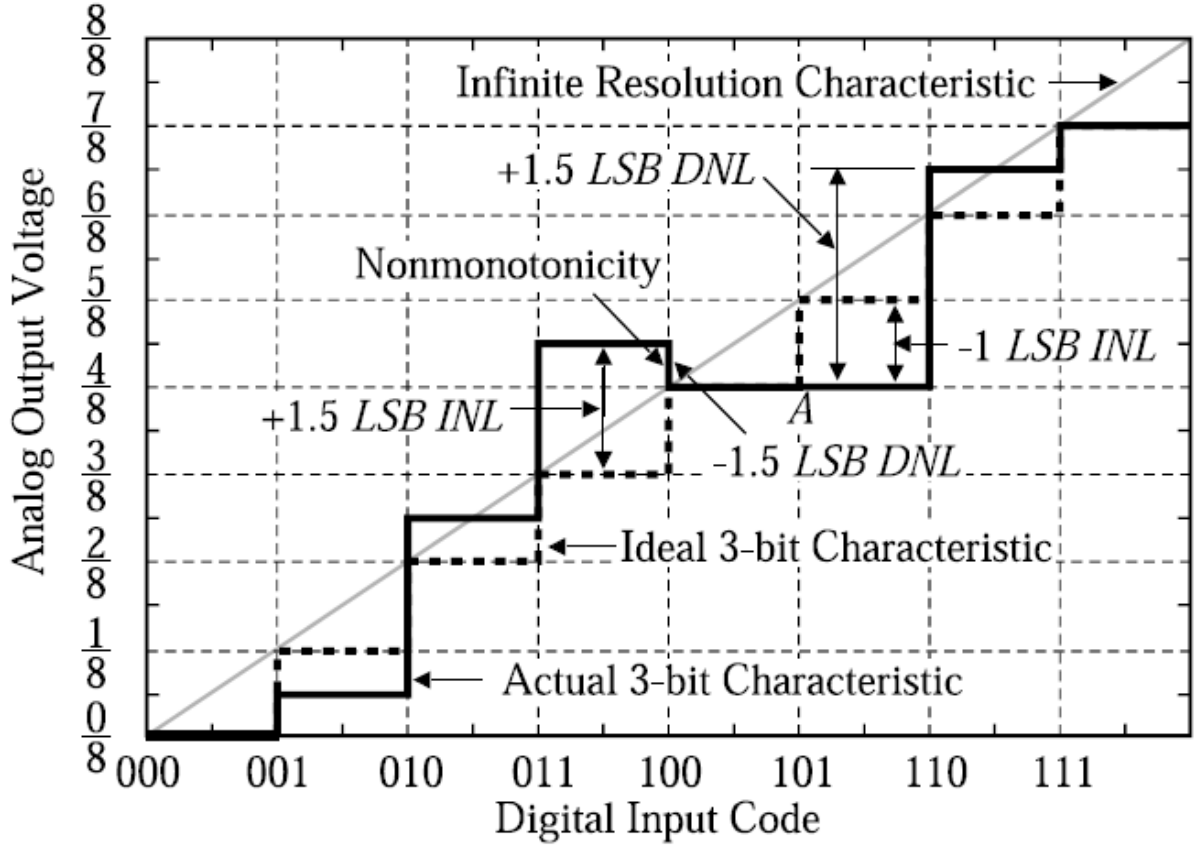
Offset Error in a 3-bit DAC



Gain Error in a 3-bit DAC

Integral and Differential Nonlinearity

- *Integral Nonlinearity* (*INL*) is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*).
- *Differential Nonlinearity* (*DNL*) is a measure of the separation between adjacent levels measured at each vertical jump (% or *LSB*).



- Monotonicity: Whenever digital input codes of the DAC increases, if the analog output never exhibits to decrease, then the converter gives monotonic characteristics

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DYNAMIC CHARACTERISTICS OF DIGITAL-ANALOG CONVERTERS

Dynamic characteristics include the influence of time.

Definitions

- *Conversion speed* is the time it takes for the DAC to provide an analog output when the digital input word is changed.

  Factor that influence the conversion speed:

  Parasitic capacitors (would like all nodes to be low impedance)

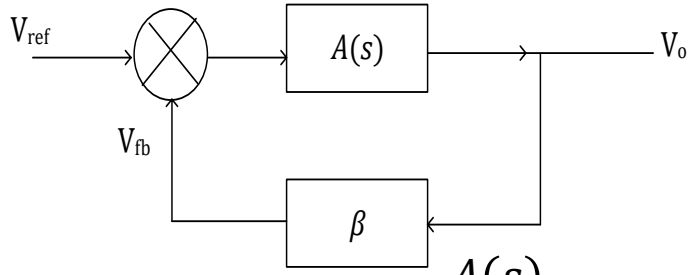
  Op amp gainbandwidth

  Op amp slew rate

- *Gain error* of an op amp is the difference between the desired and actual output voltage of the op amp (can have both a static and dynamic influence)

$$\text{Actual Gain} = \text{Ideal Gain} \times \left(\frac{\text{Loop Gain}}{1 + \text{Loop Gain}}\right)$$

$$\text{Gain error} = \frac{\text{Ideal Gain-Actual Gain}}{\text{Ideal Gain}} = \frac{1}{1+\text{Loop Gain}}$$



$$Actual\ Gain = \frac{A(s)}{1 + \beta\, A(s)}$$

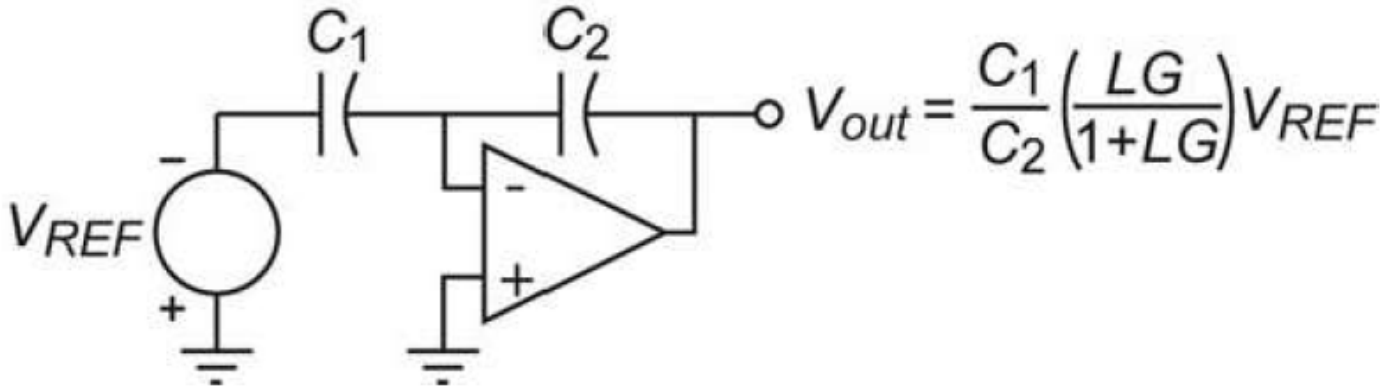
$$Ideal\ Gain = \frac{1}{\beta}$$

Example

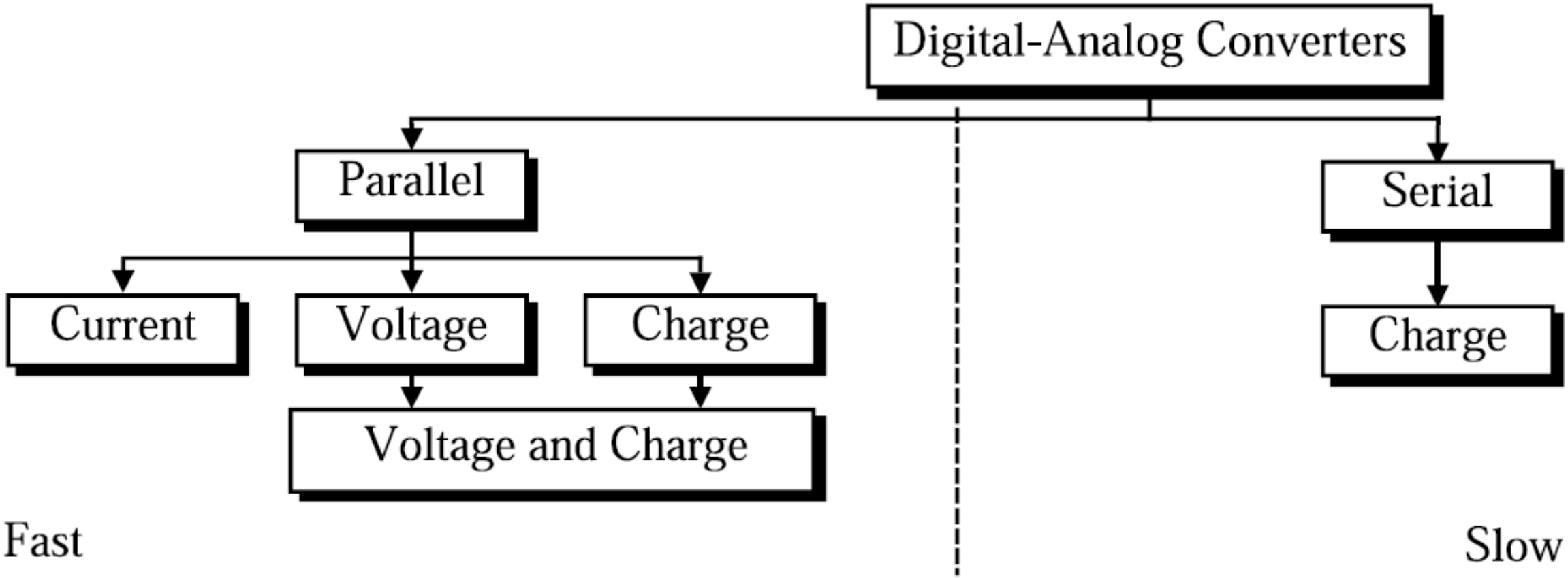
Assume that a DAC using an op amp in the inverting configuration with $C_1 = C_2$ and $A_{vd}(0) = 1000$. Find out the gain error.

Solution

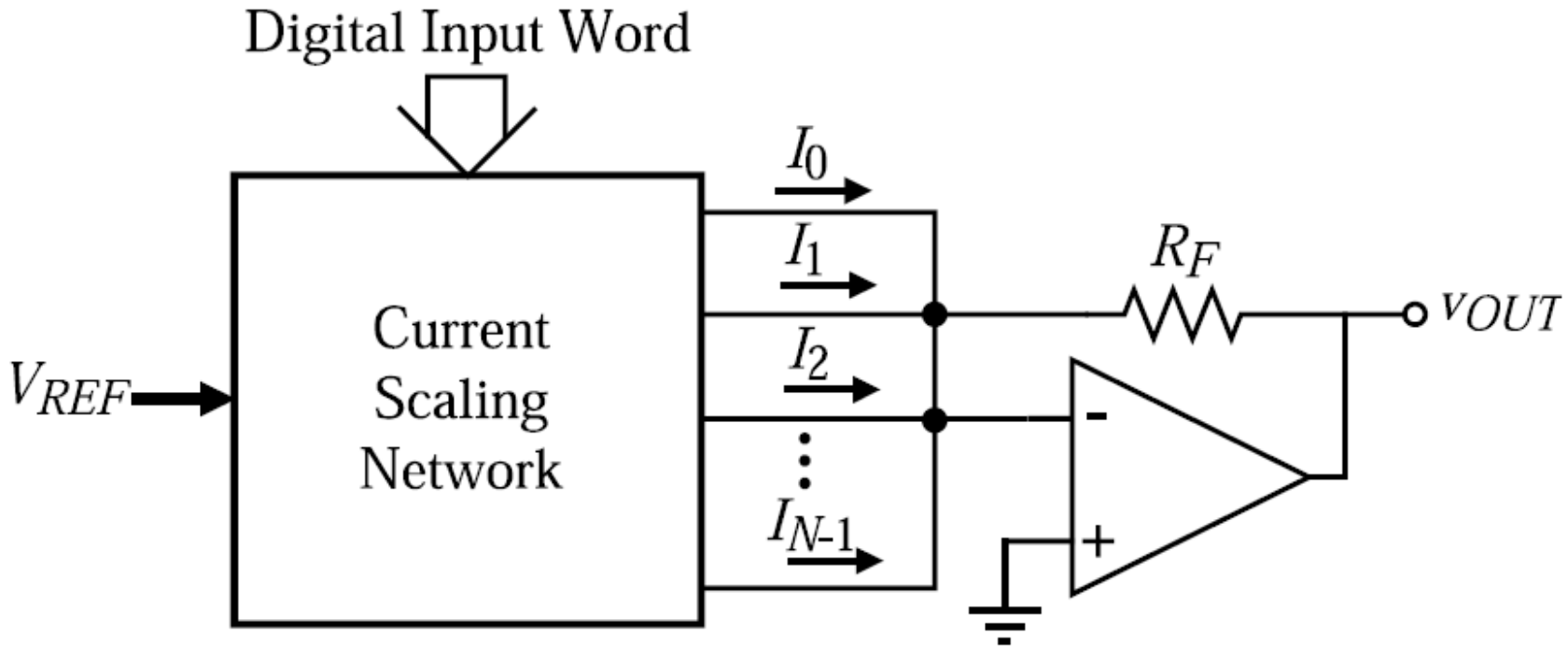
The loop gain of the inverting configuration is $LG = \frac{C_2}{C_1+C_2} A_{vd}(0) = 0.5 \cdot 1000 = 500$. The gain error is therefore $1/501 \approx 0.002$.



Classification of Digital-Analog Converters



General Current Scaling DACs



The output voltage can be expressed as

$$V_{OUT} = -R_F(I_0 + I_1 + I_2 + \cdots + I_{N-1})$$

where the currents I_0, I_1, I_2, ... are binary weighted currents.

Binary-Weighted Resistor DAC

Circuit:

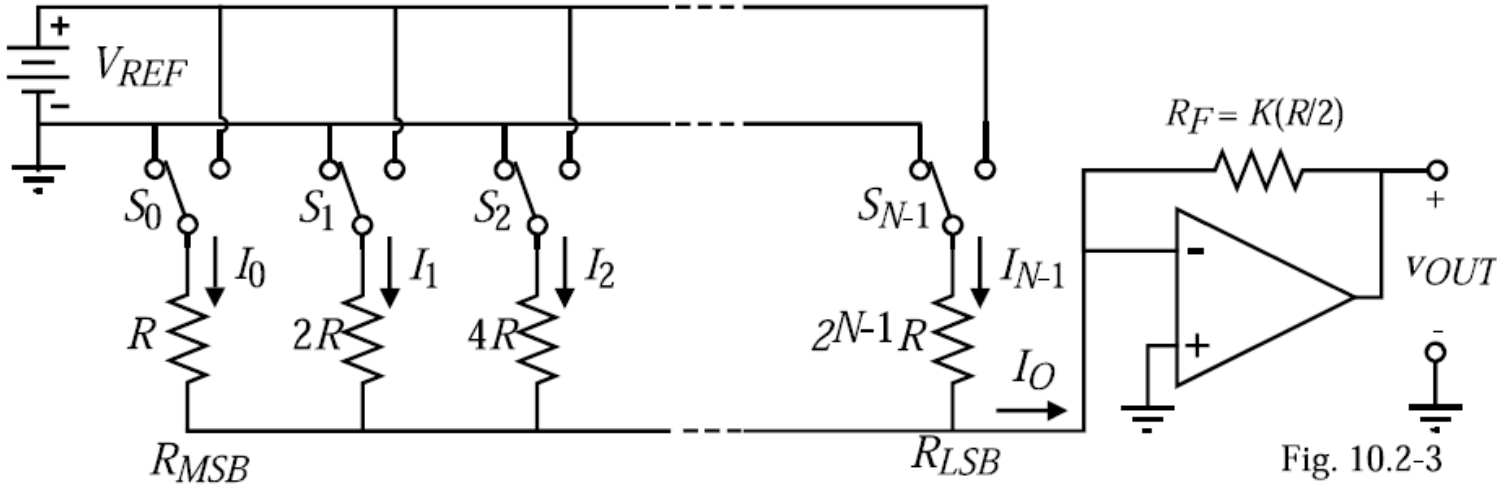


Fig. 10.2-3

Comments:

1.) R_F can be used to scale the gain of the DAC. If $R_F = KR/2$, then

$$v_{OUT} = -R_F I_O = \frac{-KR}{2}\left(\frac{b_0}{R} + \frac{b_1}{2R} + \frac{b_2}{4R} + \cdots + \frac{b_{N-1}}{2^{N-1}R}\right) V_{REF} \Rightarrow v_{OUT} = -K\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-1}}{2^N}\right) V_{REF}$$

where b_i is 1 if switch S_i is connected to V_{REF} or 0 if switch S_i is connected to ground.

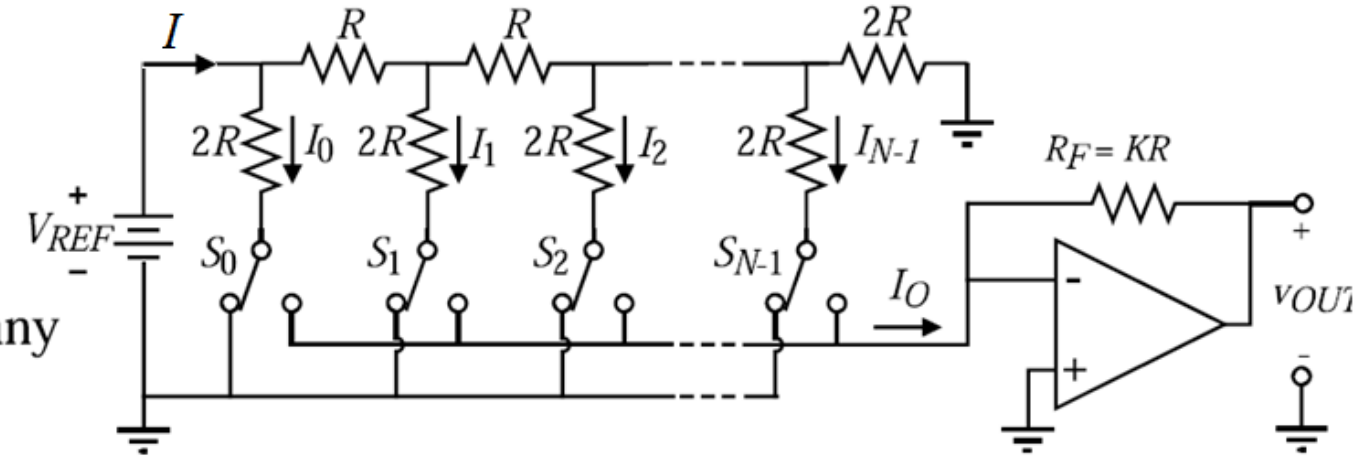
2.) Component spread value $= \dfrac{R_{MSB}}{R_{LSB}} = \dfrac{R}{2^{N-1}R} = \dfrac{1}{2^{N-1}}$

3.) Attributes:

Insensitive to parasitics $\Rightarrow$ fast	Large component spread value
Trimming required for large values of N	Nonmonotonic

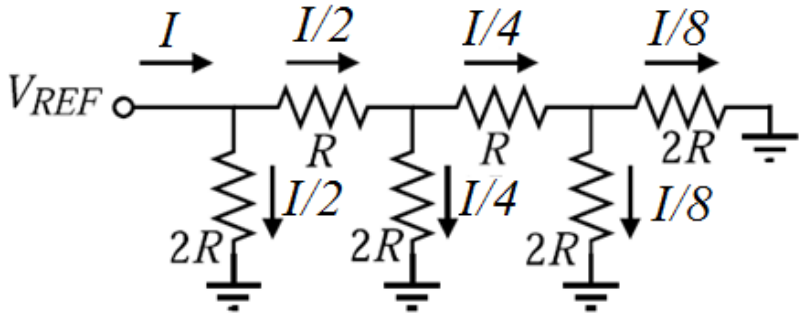
R-2R Ladder Implementation of the Binary Weighted Resistor DAC

Use of the R-2R concept to avoid large element spreads:



How does the R-2R ladder work?

"The resistance seen to the right of any of the vertical $2R$ resistors is $2R$."



$$I = \frac{V_{REF}}{R}, I_0 = \frac{V_{REF}}{2R}, I_1 = \frac{V_{REF}}{2^2R}, I_2 = \frac{V_{REF}}{2^3R}, I_{N-1} = \frac{V_{REF}}{2^NR}$$

$$v_{OUT} = -R_F I_O = -R_F[b_o I_o + b_1 I_1 + b_2 I_2 + \cdots + b_{N-1} I_{N-1}]$$

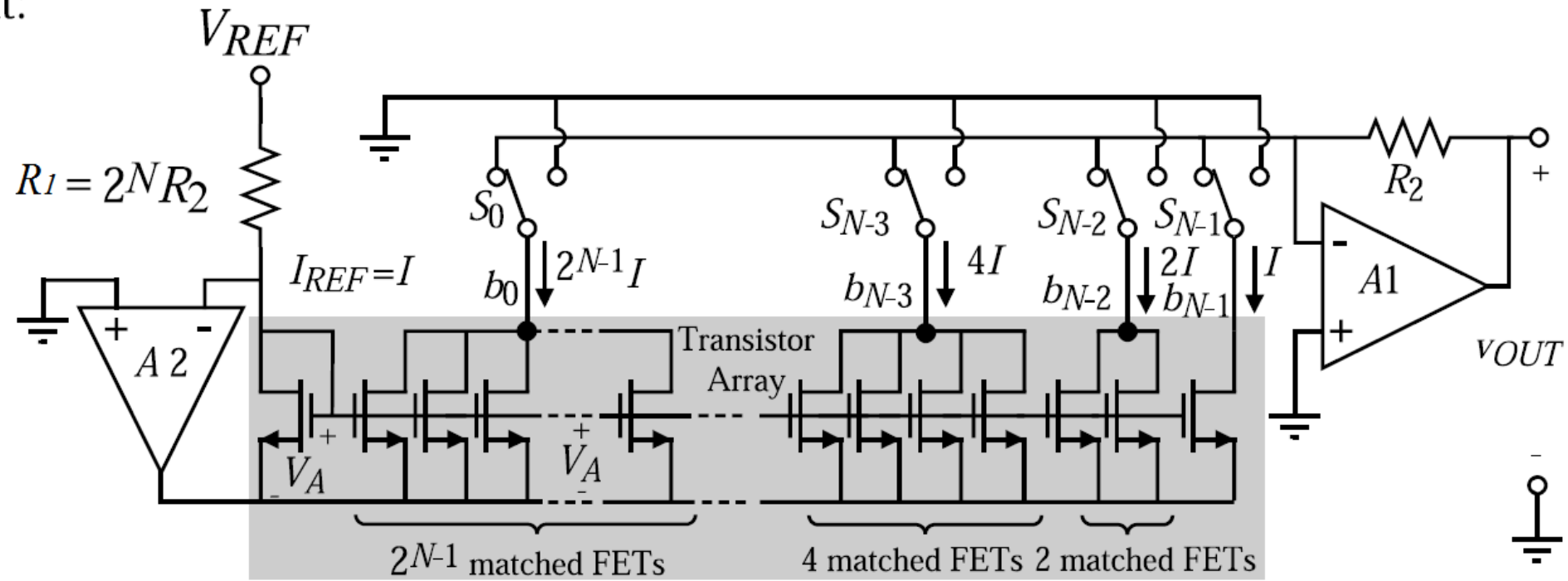
$$v_{OUT} = -KV_{REF}\left[\frac{b_0}{2^1} + \frac{b_1}{2^2} + \frac{b_2}{2^3} + \cdots + \frac{b_{N-1}}{2^N}\right]$$

Attributes:

- Not sensitive to parasitics (currents through the resistors never change as S_i is varied)
- Small element spread. Resistors made from same unit ($2R$ consist of two in series or R consists of two in parallel)
- Not monotonic

Current Scaling Using Binary Weighted MOSFET Current Sinks

Circuit:



Operation:

$$v_{OUT} = R_2(b_{N-1}\cdot I + b_{N-2}\cdot 2I + b_{N-3}\cdot 4I + \cdots + b_0\cdot 2^{N-1}\cdot I)$$

If $I = I_{REF} = \dfrac{V_{REF}}{2^N R_2}$, then $v_{OUT} = \left(\dfrac{b_0}{2} + \dfrac{b_1}{4} + \dfrac{b_2}{8} + \cdots + \dfrac{b_{N-3}}{2^{N-2}} + \dfrac{b_{N-2}}{2^{N-1}} + \dfrac{b_{N-1}}{2^N}\right) V_{REF}$

Attributes:

Fast (no floating nodes) and not monotonic

Accuracy of MSB greater than LSBs

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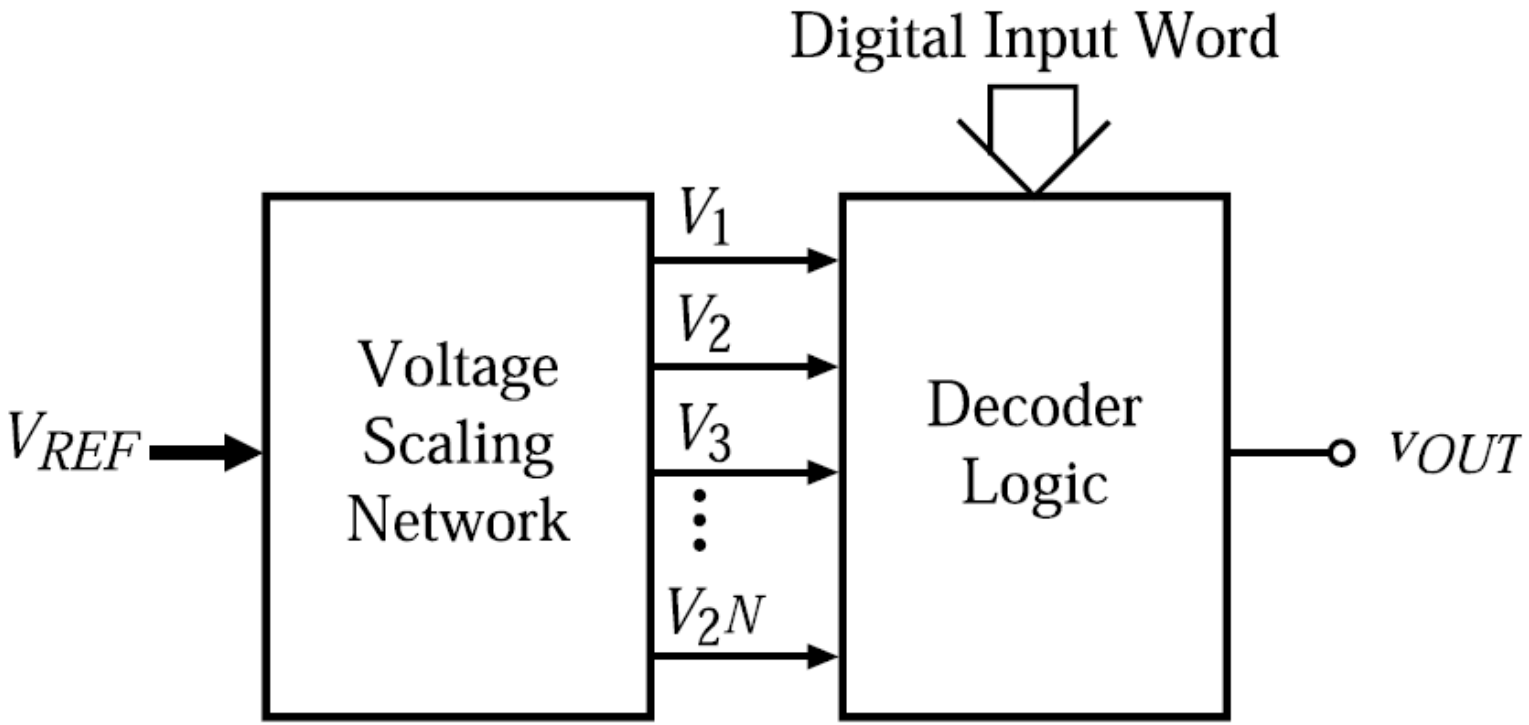
VOLTAGE SCALING DIGITAL-ANALOG CONVERTERS

General Voltage Scaling Digital Analog Converter



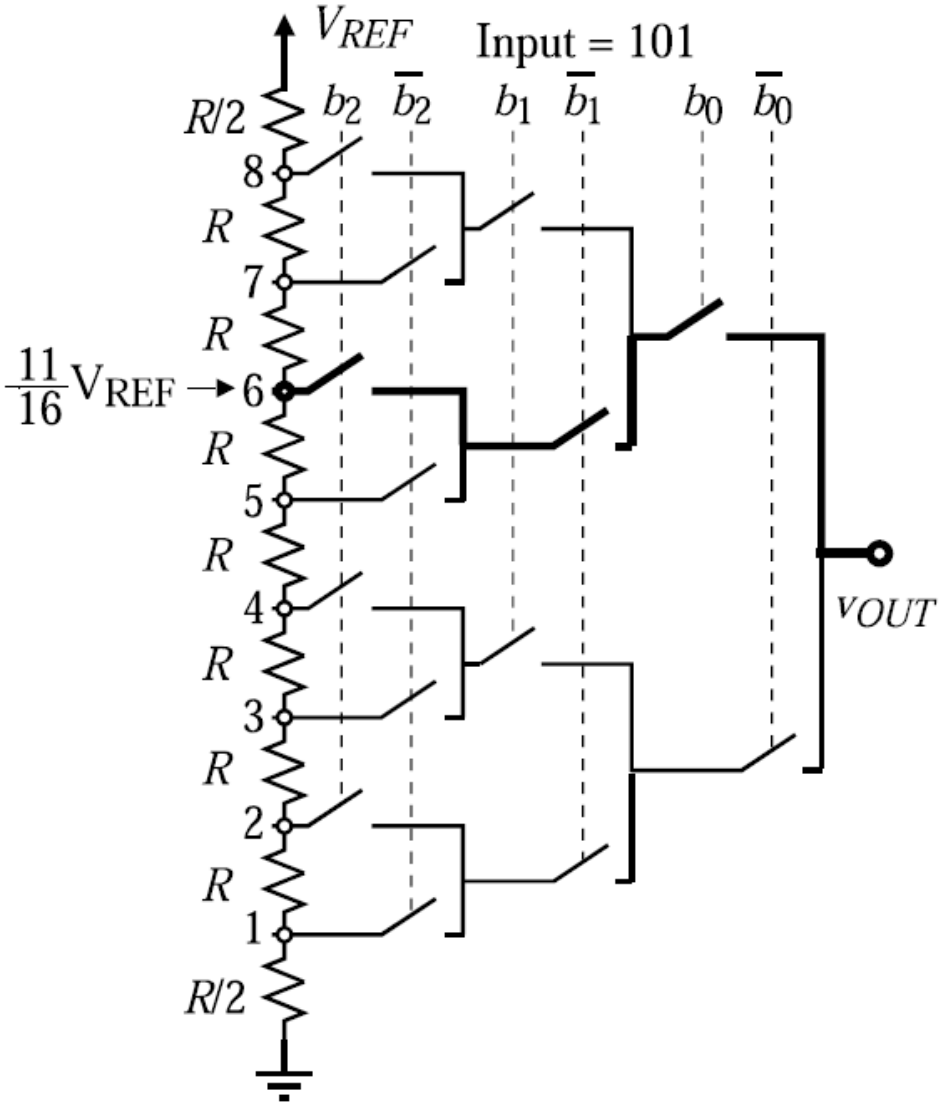
Operation:

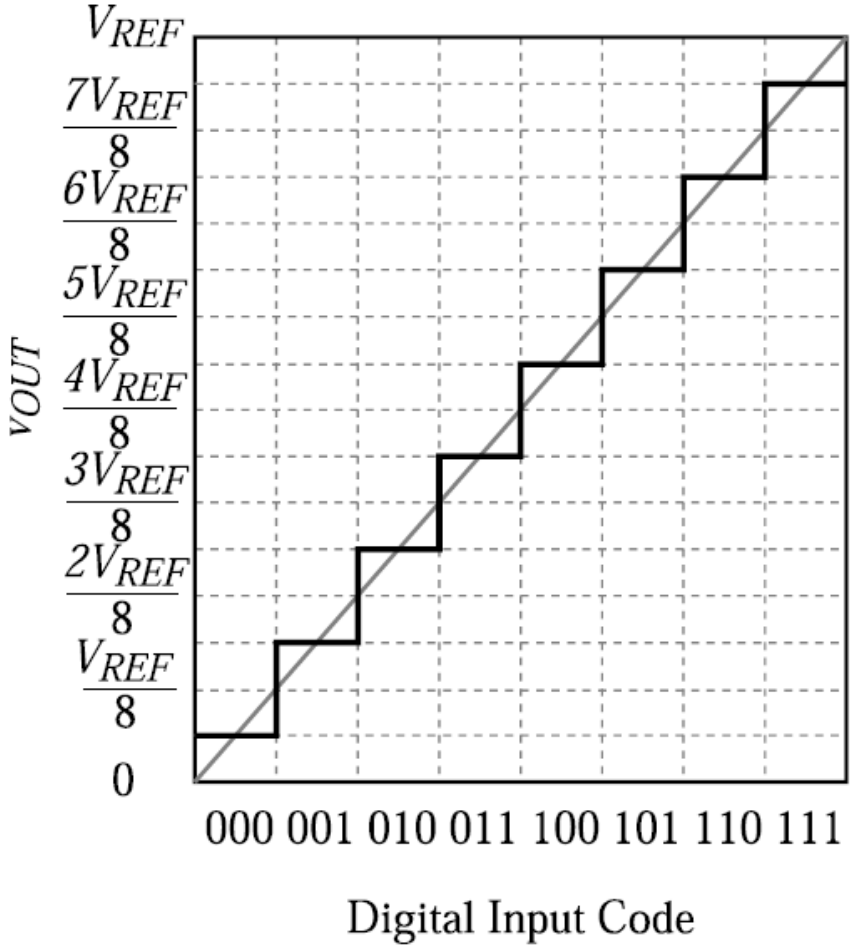
Creates all possible values of the analog output then uses a decoding network to determine which voltage to select based on the digital input word.

3-Bit Voltage Scaling Digital-Analog Converter

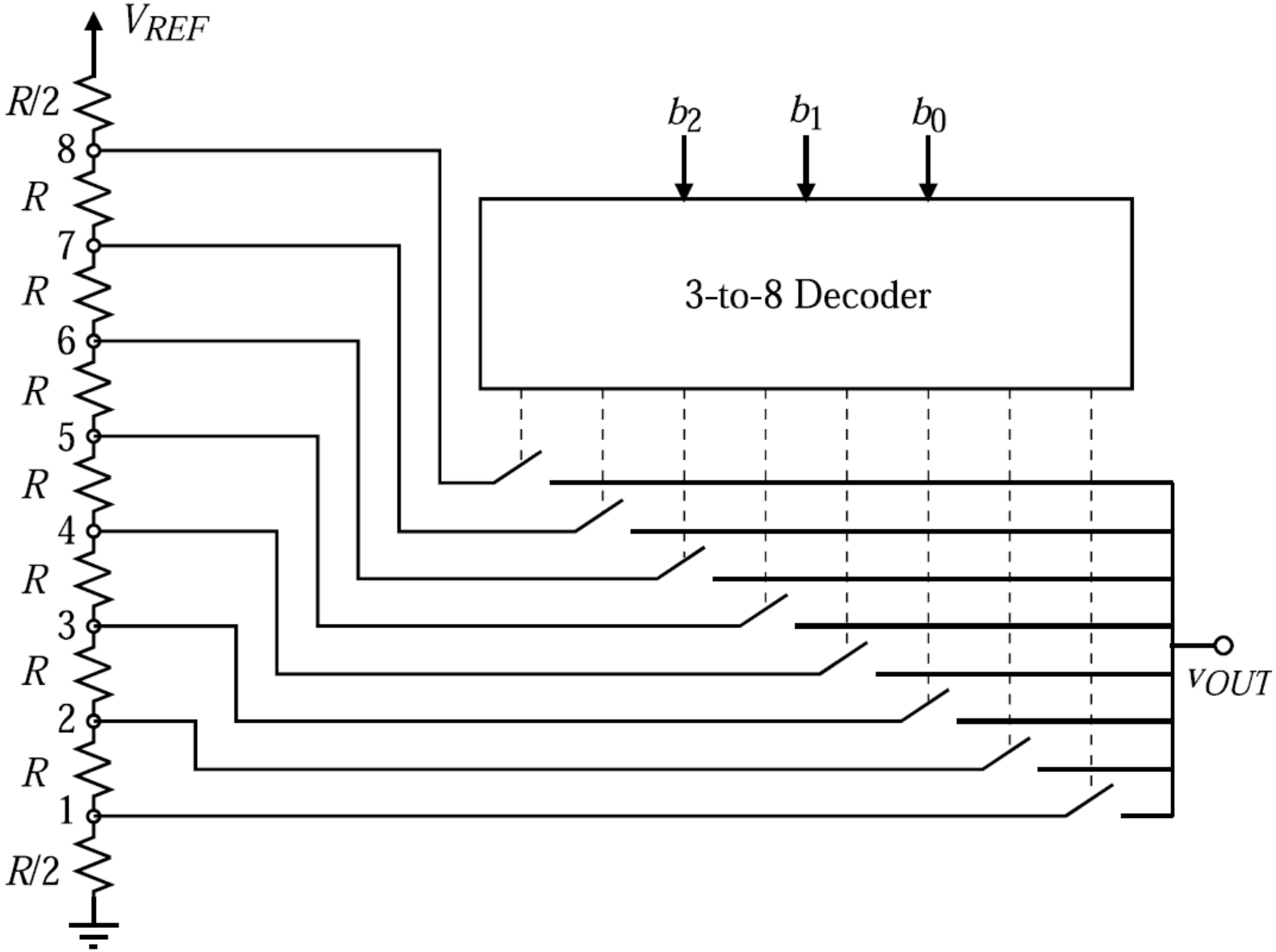
Attributes:

- Guaranteed monotonic
- Compatible with CMOS technology
- Large area if N is large
- Sensitive to parasitics
- Requires a buffer
- Large current can flow through the resistor string.





Alternate Realization of the 3-Bit Voltage Scaling DAC



CHARGE SCALING DIGITAL-ANALOG CONVERTERS

General Charge Scaling Digital-Analog Converter

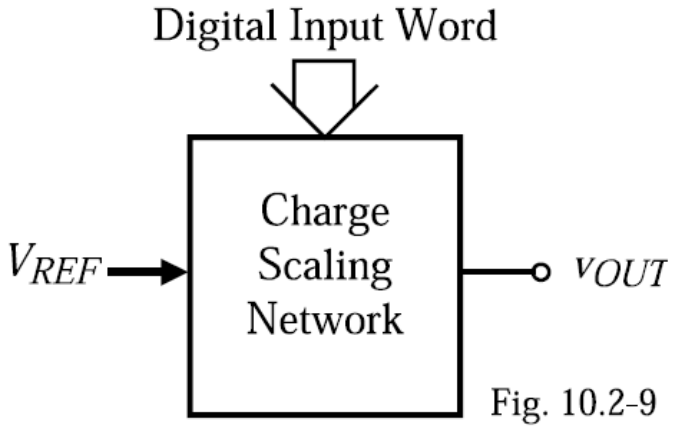
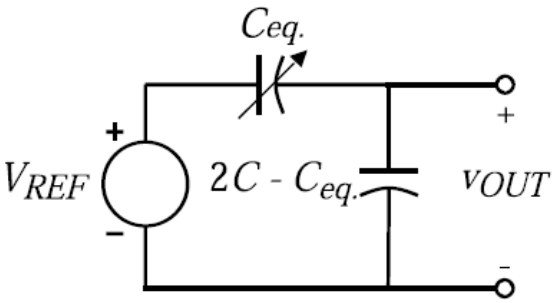


Fig. 10.2-9

General principle is to capacitively attenuate the reference voltage.



$$v_{OUT} = \frac{V_{REF} C_{eq}}{2C}$$

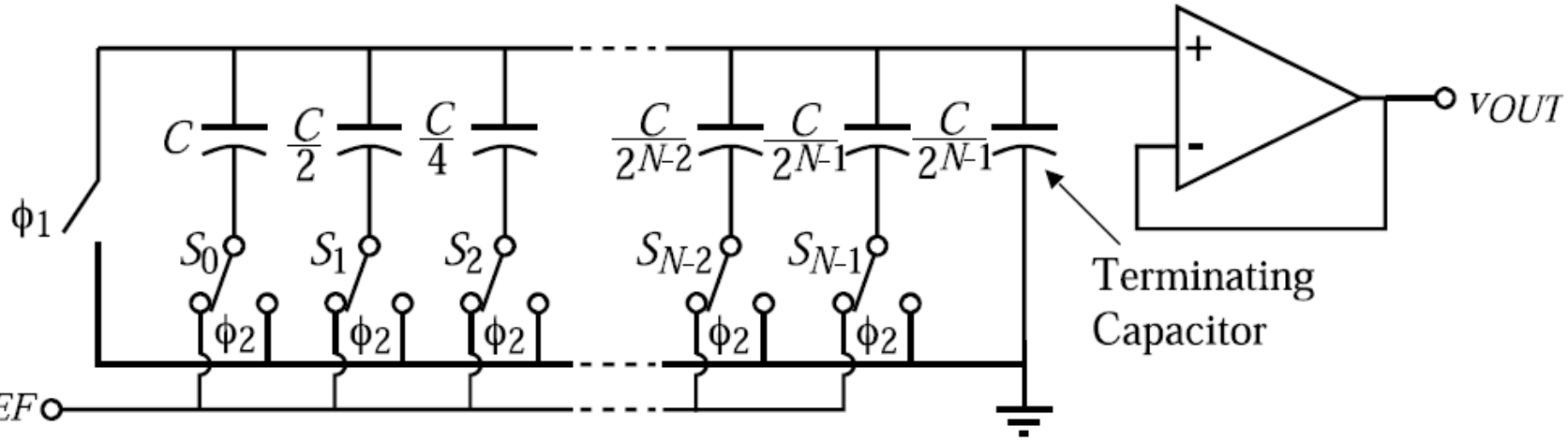
$$C_{eq} = \frac{b_0 C}{2^0} + \frac{b_1 C}{2^1} + \frac{b_2 C}{2^2} + \cdots + \frac{b_{N-1} C}{2^{N-1}}$$

$$v_{OUT} = \frac{V_{REF}}{C}\left[\frac{b_0 C}{2^1} + \frac{b_1 C}{2^2} + \frac{b_2 C}{2^3} + \cdots + \frac{b_{N-1} C}{2^N}\right]$$

$$v_{OUT} = V_{REF}\left[\frac{b_0}{2^1} + \frac{b_1}{2^2} + \frac{b_2}{2^3} + \cdots + \frac{b_{N-1}}{2^N}\right]$$

Binary-Weighted, Charge Scaling DAC

Circuit:



Operation:

1.) All switches connected to ground during ϕ_1.

2.) Switch S_i closes to V_{REF} if $b_i = 1$ or to ground if $b_i = 0$.

Equating the charge in the capacitors gives,

$$v_{OUT} = V_{REF}\left[\frac{b_0}{2^1} + \frac{b_1}{2^2} + \frac{b_2}{2^3} + \cdots + \frac{b_{N-1}}{2^N}\right]$$

Attributes:

- Sensitive to parasitics
- Not monotonic

SERIAL DIGITAL-ANALOG CONVERTERS

Serial DACs

- Typically require one clock pulse to convert one bit

Charge Redistribution DAC

Implementation:

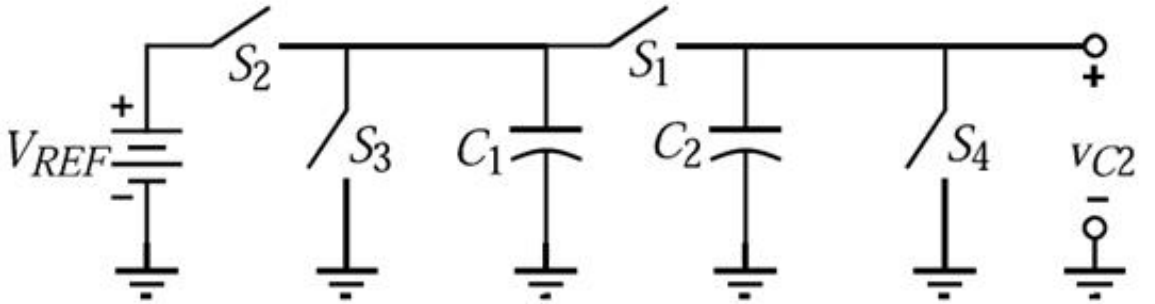


Fig. 10.4-1

Operation:

Switch S_4 is used at the beginning of the conversion process to initially discharge C_2

Switch S_2 precharges C_1 to V_{REF} if the ith bit, b_i, is a 1

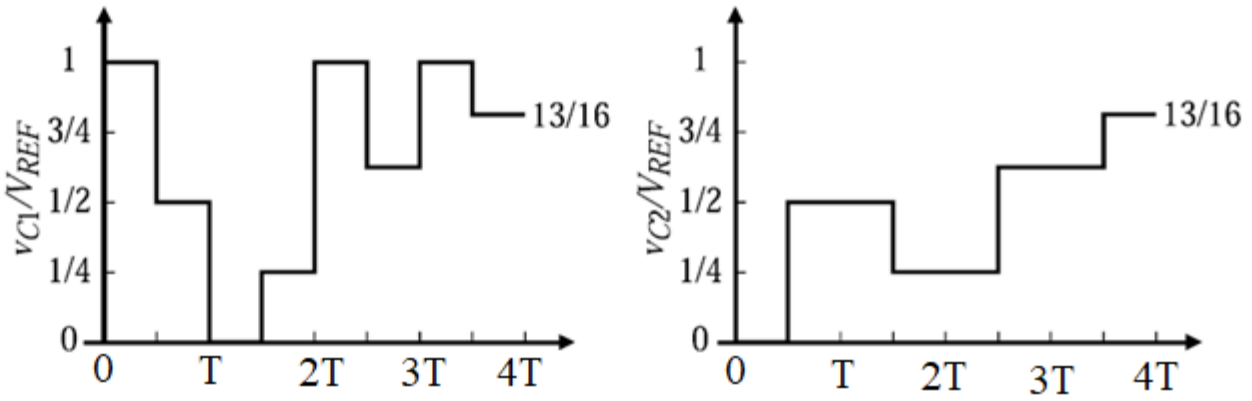
Switch S_3 discharges C_1 to zero if the ith bit, b_i, is a 0

Switch S_1 is the redistribution switch that parallels C_1 and C_2 sharing their charge

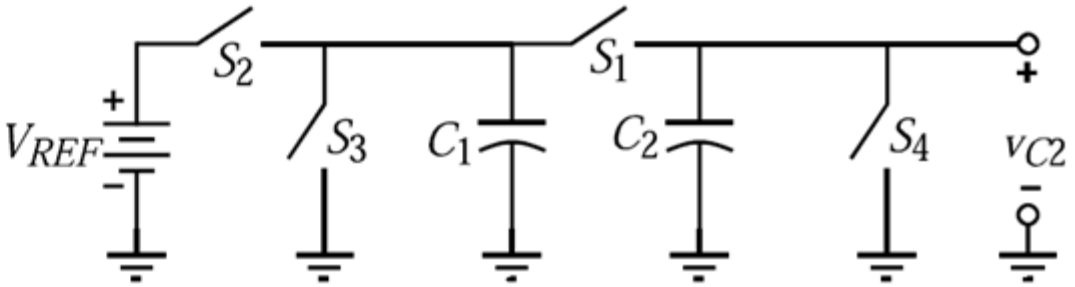
Conversion always begins with the LSB bit and goes to the MSB bit.

Example 350-7 - Operation of the Serial, Charge Redistribution DAC

Assume that $C_1 = C_2$ and that the digital word to be converted is given as $b_0 = 1$, $b_1 = 1$, $b_2 = 0$, and $b_3 = 1$. Follow through the sequence of events that result in the conversion of this digital input word.



Solution



1.) S_4 closes setting $v_{C2} = 0$.
2.) $b_3 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
3.) Switch S_1 is closed causing $v_{C1} = v_{C2} = 0.5\,V_{REF}$.
4.) $b_2 = 0$, closes switch S_3, causing $v_{C1} = 0$V.
5.) S_1 closes, the voltage across both C_1 and C_2 is $0.25\,V_{REF}$.
6.) $b_1 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
7.) S_1 closes, the voltage across both C_1 and C_2 is $(1+0.25)/2\,V_{REF} = 0.625\,V_{REF}$.
8.) $b_0 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
9.) S_1 closes, the voltage across both C_1 and C_2 is $(0.625 + 1)/2\,V_{REF} = 0.8125\,V_{REF} = (13/16)\,V_{REF}$.

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EXTENDING THE RESOLUTION OF PARALLEL DIGITAL-ANALOG CONVERTERS

Background

Technique:

Divide the total resolution N into k smaller sub-DACs each with a resolution of $\frac{N}{k}$.

Result:

Smaller total area.

More resolution because of reduced largest to smallest component spread.

Approaches:

- Combination of similarly scaled subDACs
  - Divider approach (scale the analog output of the subDACs)
  - Subranging approach (scale the reference voltage of the subDACs)
- Combination of differently scaled subDACs

COMBINATION OF SIMILARLY SCALED SUBDACs

Analog Scaling - Divider Approach

Example of combining a *m*-bit and *k*-bit subDAC to form a *m*+*k*-bit DAC.

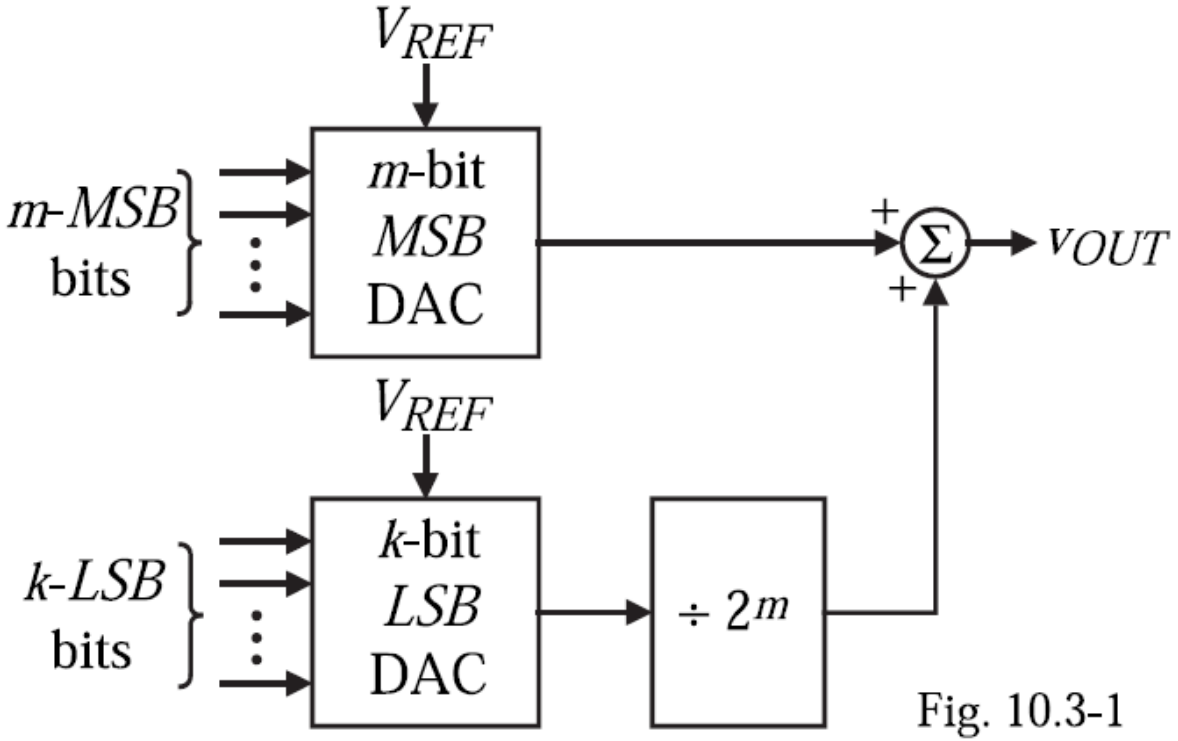


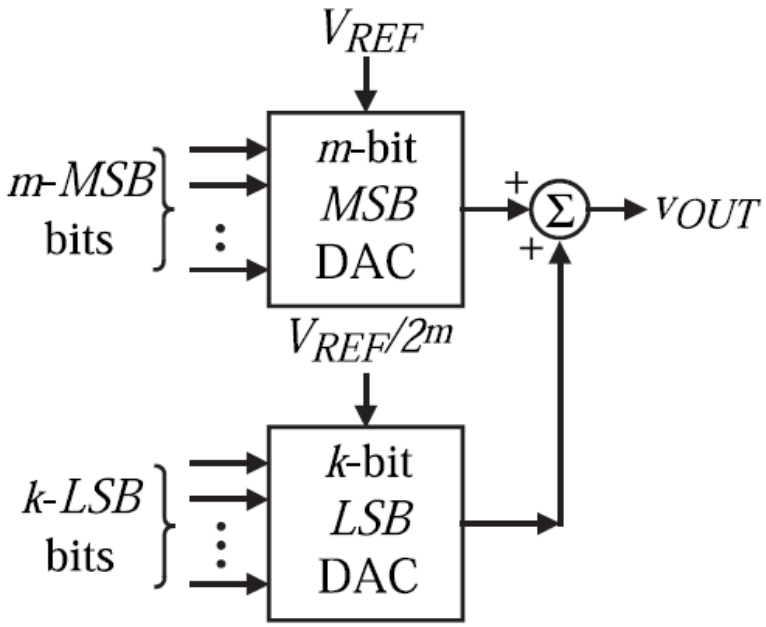
Fig. 10.3-1

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m-1}}{2^m}\right) V_{REF} + \left(\frac{1}{2^m}\right)\left(\frac{b_m}{2} + \frac{b_{m+1}}{4} + \cdots + \frac{b_{m+k-1}}{2^k}\right) V_{REF}$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \cdots + \frac{b_{m+k-1}}{2^{m+k}}\right) V_{REF}$$

Reference Scaling - Subranging Approach

Example of combining a *m*-bit and *k*-bit subDAC to form a *m*+*k*-bit DAC.



$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m-1}}{2^m}\right) V_{REF} + \left(\frac{b_m}{2} + \frac{b_{m+1}}{4} + \cdots + \frac{b_{m+k-1}}{2^k}\right)\left(\frac{V_{REF}}{2^m}\right)$$

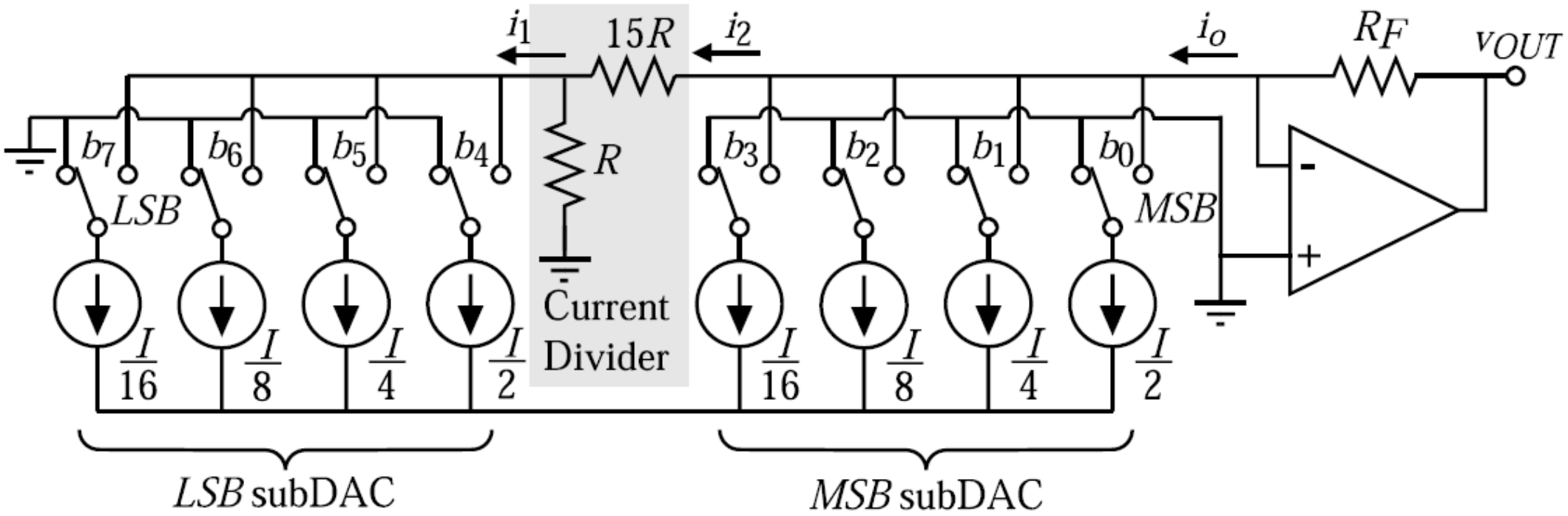
$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \cdots + \frac{b_{m+k-1}}{2^{m+k}}\right) V_{REF}$$

Accuracy considerations of this method are similar to the analog scaling approach.

Advantage: There are no dynamic limitations associated with the scaling factor of $1/2^m$.

Current Scaling Dac Using Two SubDACs

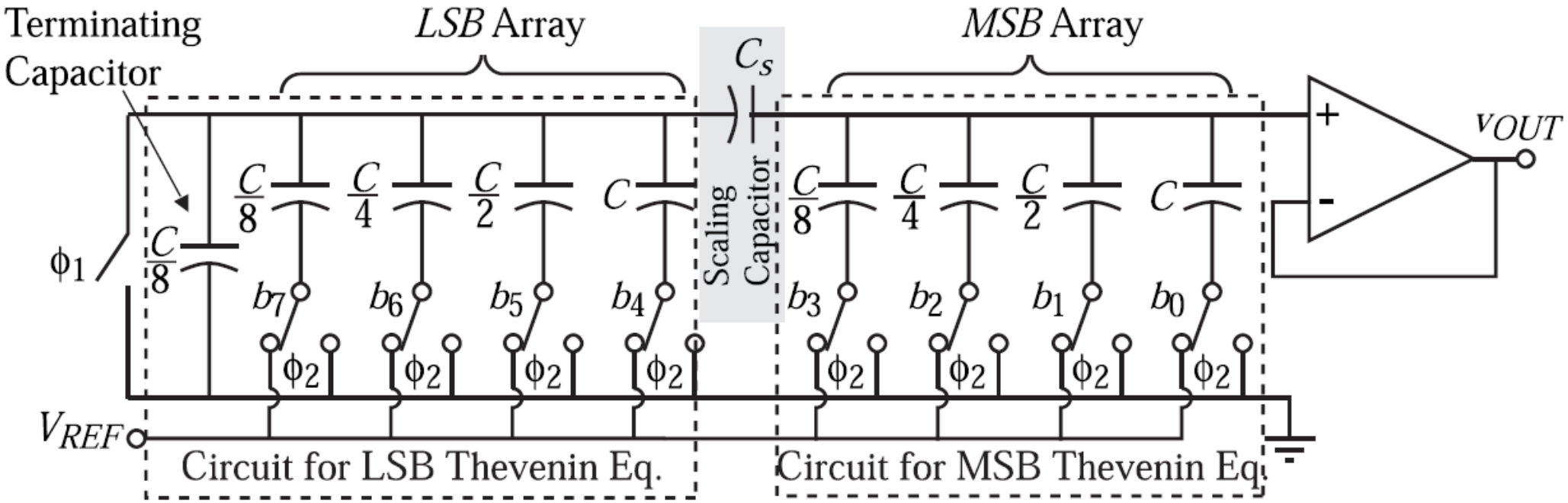
Implementation:



$$v_{OUT} = R_F I\left[\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}\right) + \frac{1}{16}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)\right]$$

Charge Scaling DAC Using Two SubDACs

Implementation:



Design of the scaling capacitor, C_s:

The series combination of C_s and the *LSB* array must terminate the *MSB* array or equal $C/8$. Therefore, we can write

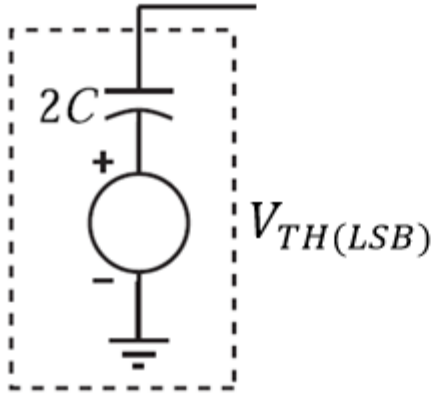
$$\frac{C}{8} = \frac{1}{\frac{1}{C_s} + \frac{1}{2C}} \quad \text{or} \quad \frac{1}{C_s} = \frac{8}{C} - \frac{1}{2C} = \frac{16}{2C} - \frac{1}{2C} = \frac{15}{2C}$$

If all the LSB bits are zero, i.e, b_4-b_5-b_6-b_7=0000, then

$$v_{OUT(MSB)} = V_{REF}\left[\frac{b_0}{2^1} + \frac{b_1}{2^2} + \frac{b_2}{2^3} + \frac{b_3}{2^4}\right]$$

Thevenin equivalent of LSB array:

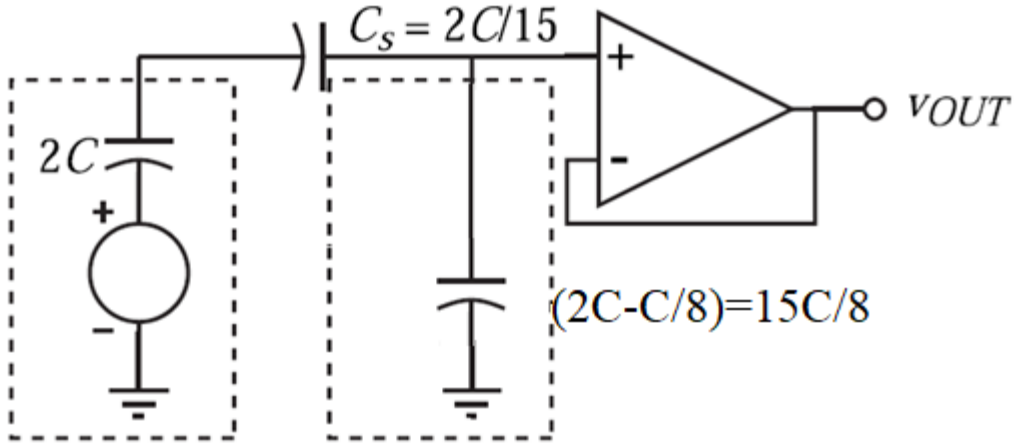
$$V_{TH(LSB)} = V_{REF}\left[\frac{b_4}{2^1} + \frac{b_5}{2^2} + \frac{b_6}{2^3} + \frac{b_7}{2^4}\right]$$



If all MSB bits are zero, i.e., b_0-b_1-b_2-b_3=0000, then

$$v_{OUT(LSB)} = V_{TH(LSB)}\left[\frac{\frac{8}{15C}}{\frac{1}{2C} + \frac{15}{2C} + \frac{8}{15C}}\right] = \frac{V_{TH(LSB)}}{16}$$

$$v_{OUT(LSB)} = \frac{V_{REF}}{16}\left[\frac{b_4}{2^1} + \frac{b_5}{2^2} + \frac{b_6}{2^3} + \frac{b_7}{2^4}\right]$$



Applying voltage superposition:

$$v_{OUT} = V_{REF}\left[\frac{b_0}{2^1} + \frac{b_1}{2^2} + \frac{b_2}{2^3} + \frac{b_3}{2^4} + \frac{b_4}{2^5} + \frac{b_5}{2^6} + \frac{b_6}{2^7} + \frac{b_7}{2^8}\right]$$

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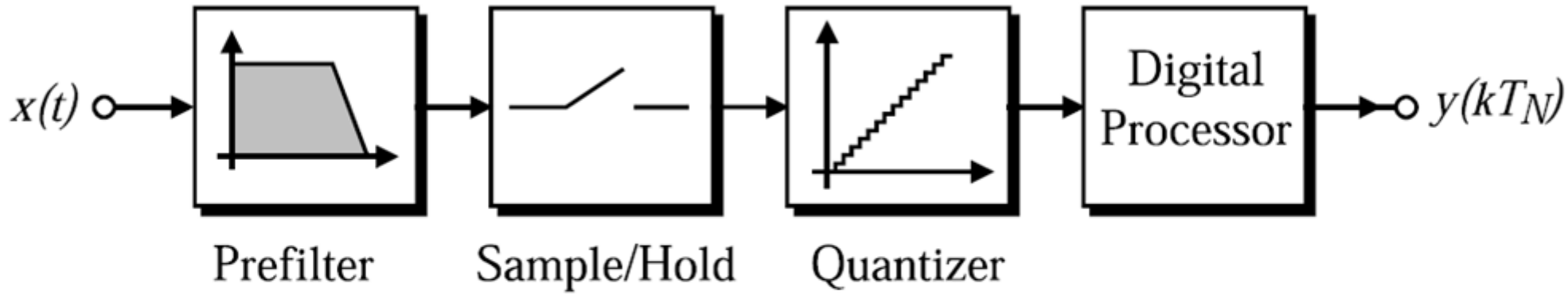
General Block Diagram of an Analog-Digital Converter



- Prefilter - Avoids the aliasing of high frequency signals back into the baseband of the ADC
- Sample-and-hold - Maintains the input analog signal constant during conversion
- Quantizer - Finds the subrange that corresponds to the sampled analog input

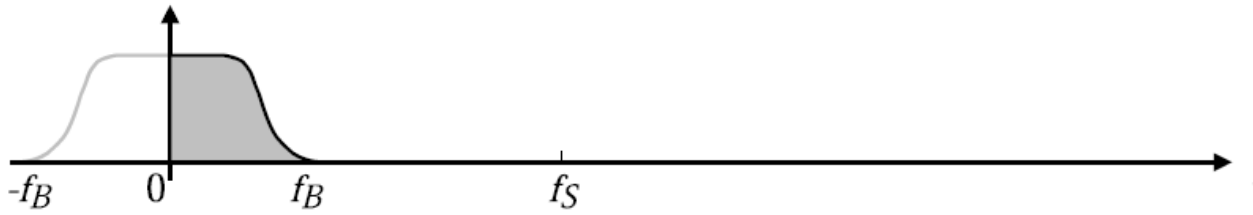
Nyquist Frequency Analog-Digital Converters

The sampled nature of the ADC places a practical limit on the bandwidth of the input signal. If the sampling frequency is f_S, and f_B is the bandwidth of the input signal, then

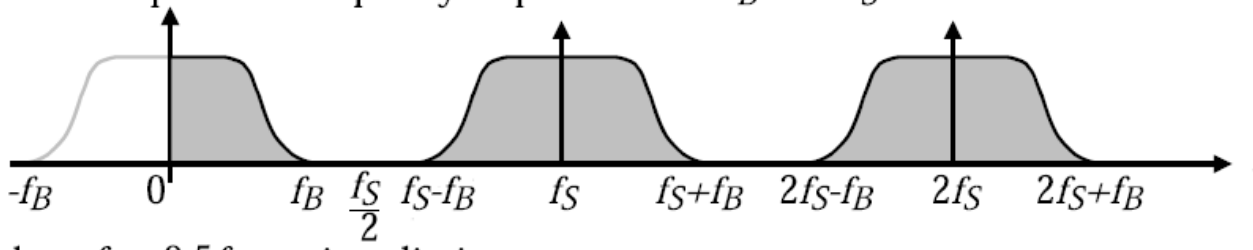
$$f_B < 0.5 f_S$$

which is simply the *Nyquist* relationship which states that to avoid aliasing, the sampling frequency must be greater than twice the highest signal frequency.

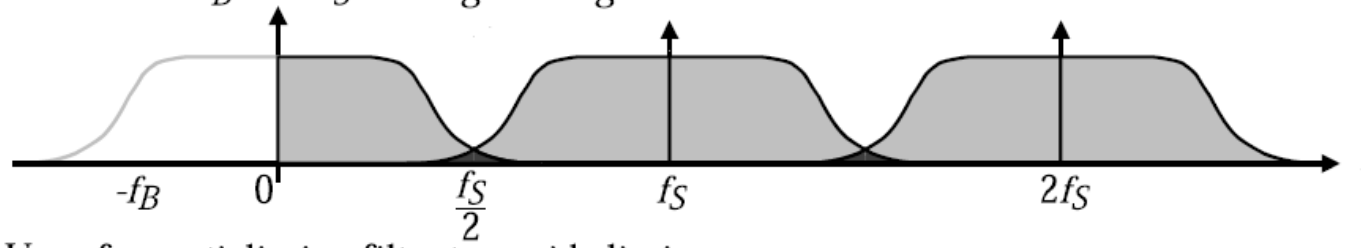
Continuous time frequency response of the analog input signal.



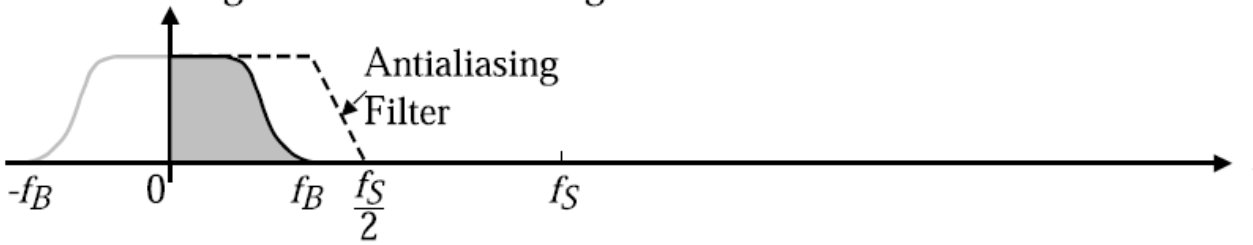
Sampled data equivalent frequency response where $f_B < 0.5 f_S$.



Case where $f_B > 0.5 f_S$ causing aliasing.



Use of an antialiasing filter to avoid aliasing.

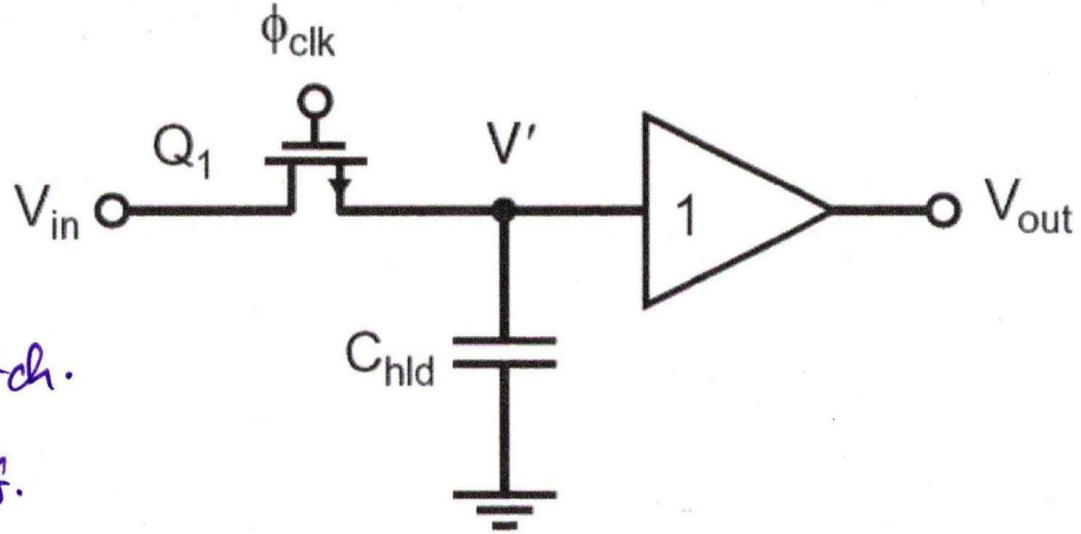


Sample and Hold

1. Important block in many data acquisition system.
2. It is used to sampled the input analog signal and hold for some time while ADC converts the digital equivalent output.
3. Two categories:
   a) S/H without feedback
   b) S/H with feedback
      - Feedback enhances the dc accuracy with sacrificing speed.

Practical S/H without feedback

- C_{hld} acts as an analog memory.
- Non-idealities :-
  a) When ϕ_{clk} is off, the charge under gate area should flow.
  b) For NMOS switch, e creates a negative glitch.



Total charge under gate = $C_{ox} . W . L . V_{eff}$.

where $V_{eff} = V_{GS} - V_{th} = (V_{DD} - V_{in} - V_{tn})$

when ϕ_{clk} goes low, half of the charges go one side and rest other side.

$$\Delta Q_{hld} = \frac{1}{2} C_{ox} W L (V_{DD} - V_{in} - V_{tn})$$

$$\Delta V' = -\frac{\Delta Q_{hld}}{C_{hld}} = -\frac{C_{ox} W L (V_{DD} - V_{in} - V_{tn})}{2 C_{hld}}$$

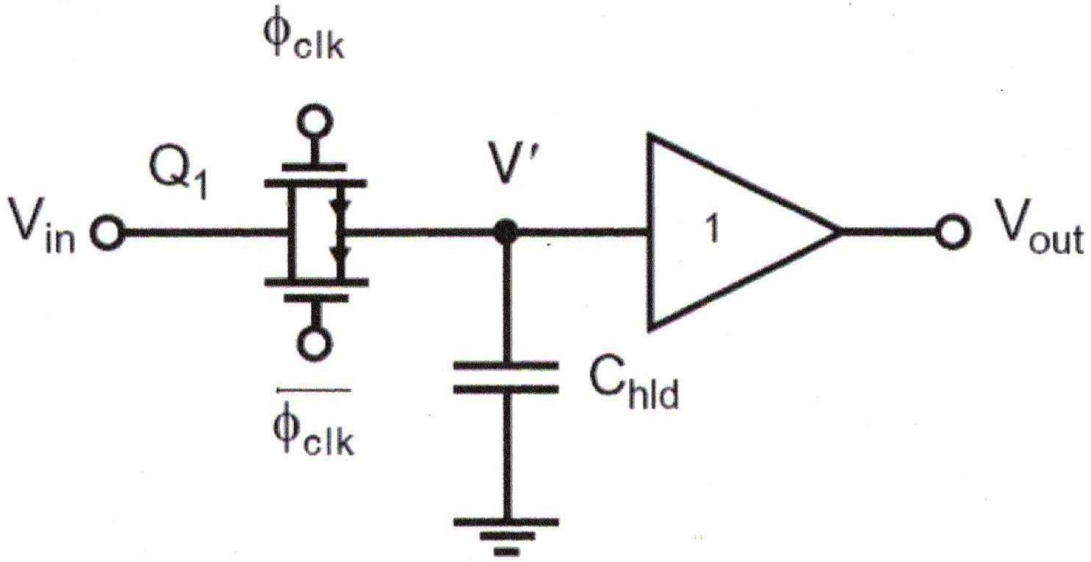
- Observations : a) $\Delta V'$ error is a signal dependent error.
  b) low W, L will reduce the error at the cost of speed.

Practical S/H without feedback

- Key idea :- Charge carrier in NMOS is electrons and in PMOS it is holes. If their sizes are same, the charge injection will cancel each other.

$$\Delta Q_{hldN} = \frac{C_{ox} WL}{2}(V_{DD} - V_{in} - V_{th})$$

$$\Delta Q_{hldP} = \frac{C_{ox} WL}{2}(0 - V_{in} - |V_{tp}|)$$



However, charge injections will be cancelled each other if $V_{in} = \frac{V_{DD}}{2}$

If V_{in} is closer to V_{DD}, charge from PMOS > charge from NMOS. $\Delta V' \uparrow$.

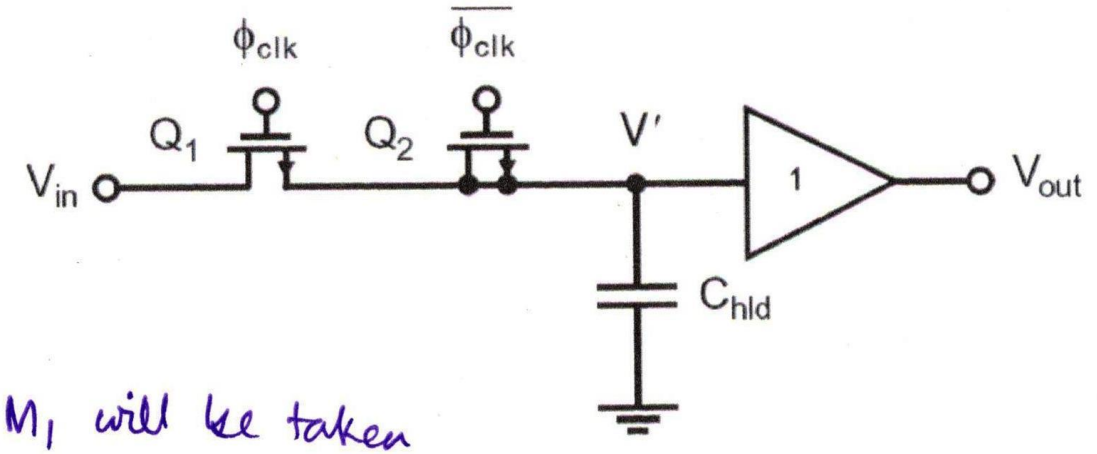
If V_{in} is closer to zero, $\Delta V' \downarrow$.

Practical S/H without feedback

Another modifications to minimise clock feedthrough / charge injection :-

Q_2 is choosen half of Q_1

Q_2 is a dummy switch.



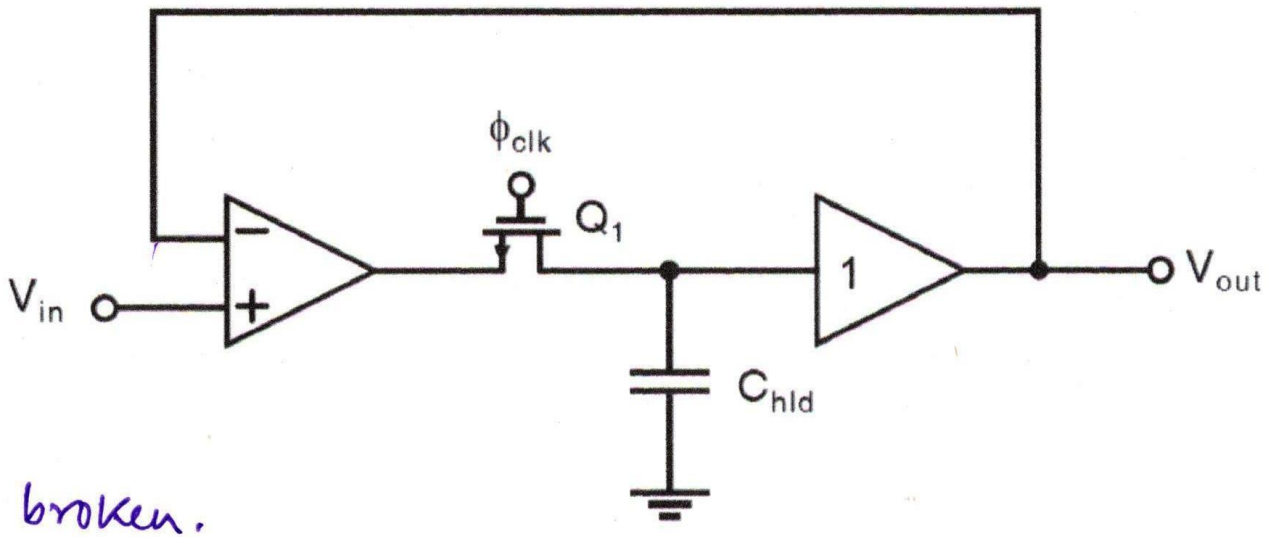
When ϕ_{clk} goes low, the charge given by M_1 will be taken out by M_2 to form the channel.

Limitations of S/H without feedback :-

Buffer introduces an offset.

Practical S/H with feedback

- Opamp increases the input impedance of S/H circuit.
- When Φ_{clk} = High, it is sample mode. dc error will be divided by op-amp gain.
- When Φ_{clk} = Low, hold mode, loop is broken.

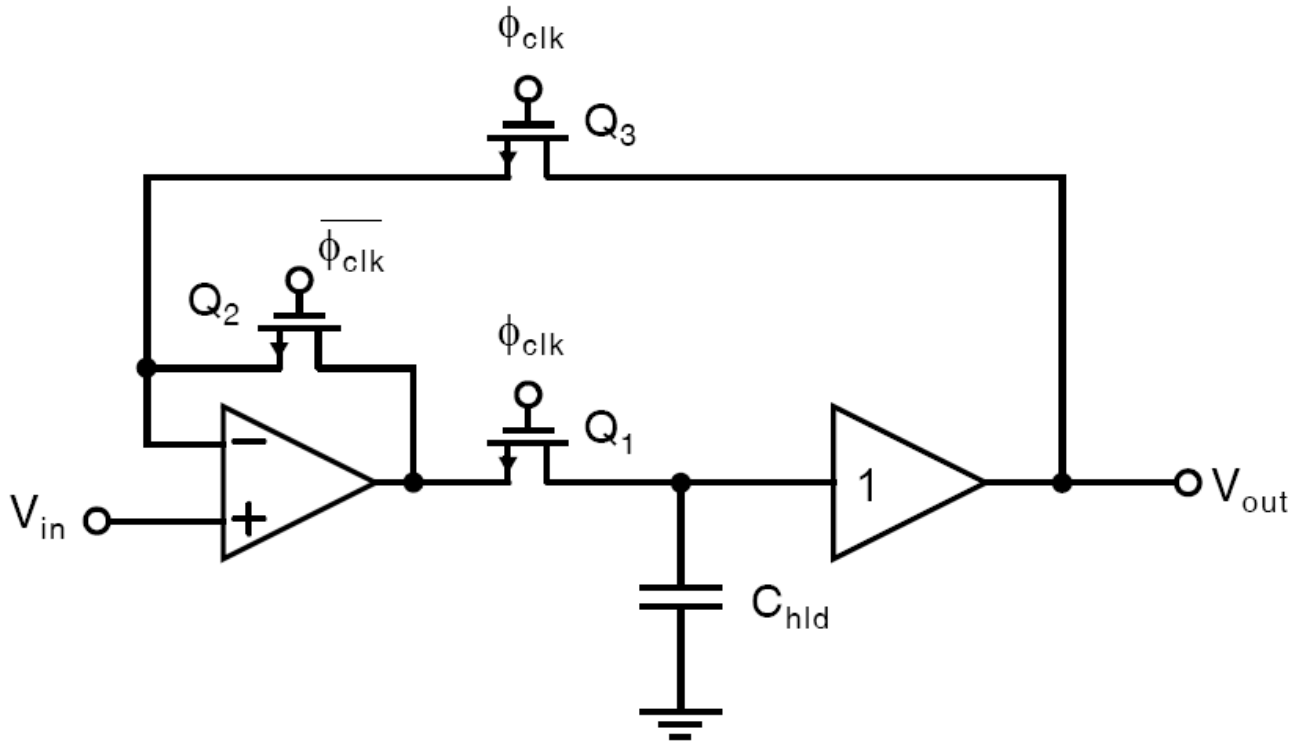


Issues:-

1) Speed of operation is degraded to guarantee the stability.
2) In hold mode, loop is broken, O/P of first op-amp saturates. In the next sample operation, slewing operation degrades the speed further.

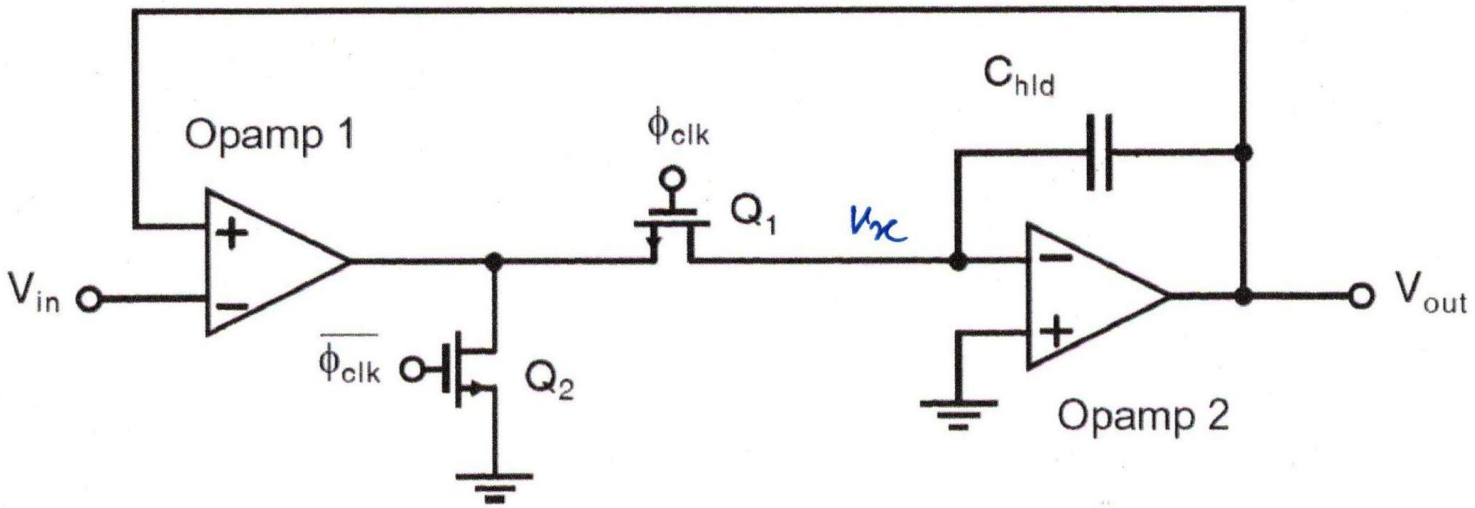
Practical S/H with feedback

Q_2 and Q_3 prevent the first op-amp from entering into saturation.



Practical S/H with feedback

C_{hld} is placed in the feedback path to form an integrator using opamp 2.



When Q_1 turns off, charge injection causes V_x to fall.

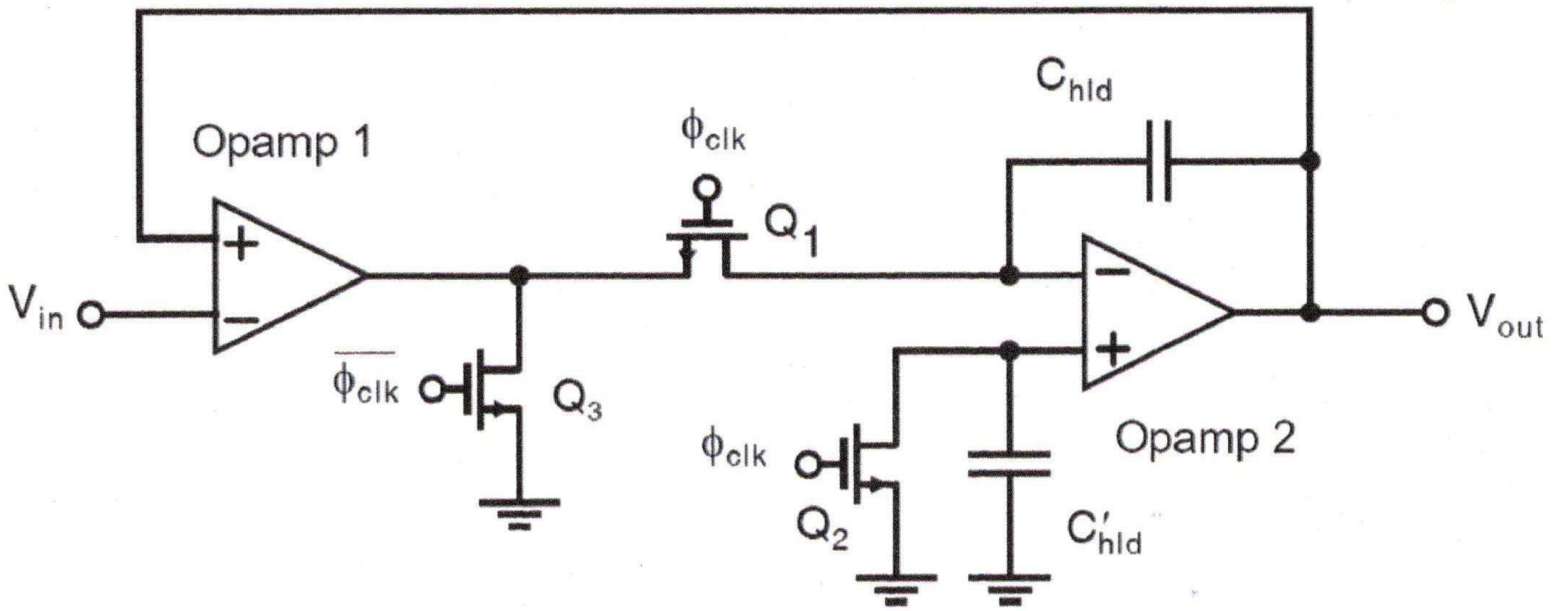
The integrator integrates this and creates an offset (dc), not distortion.

The op-amp 1 minimizes offset.

Ensuring stability is challenging.

Practical S/H with feedback

Charge injection affects both the input.
Common mode rejection of the op-amp eliminates the charge injection problem.



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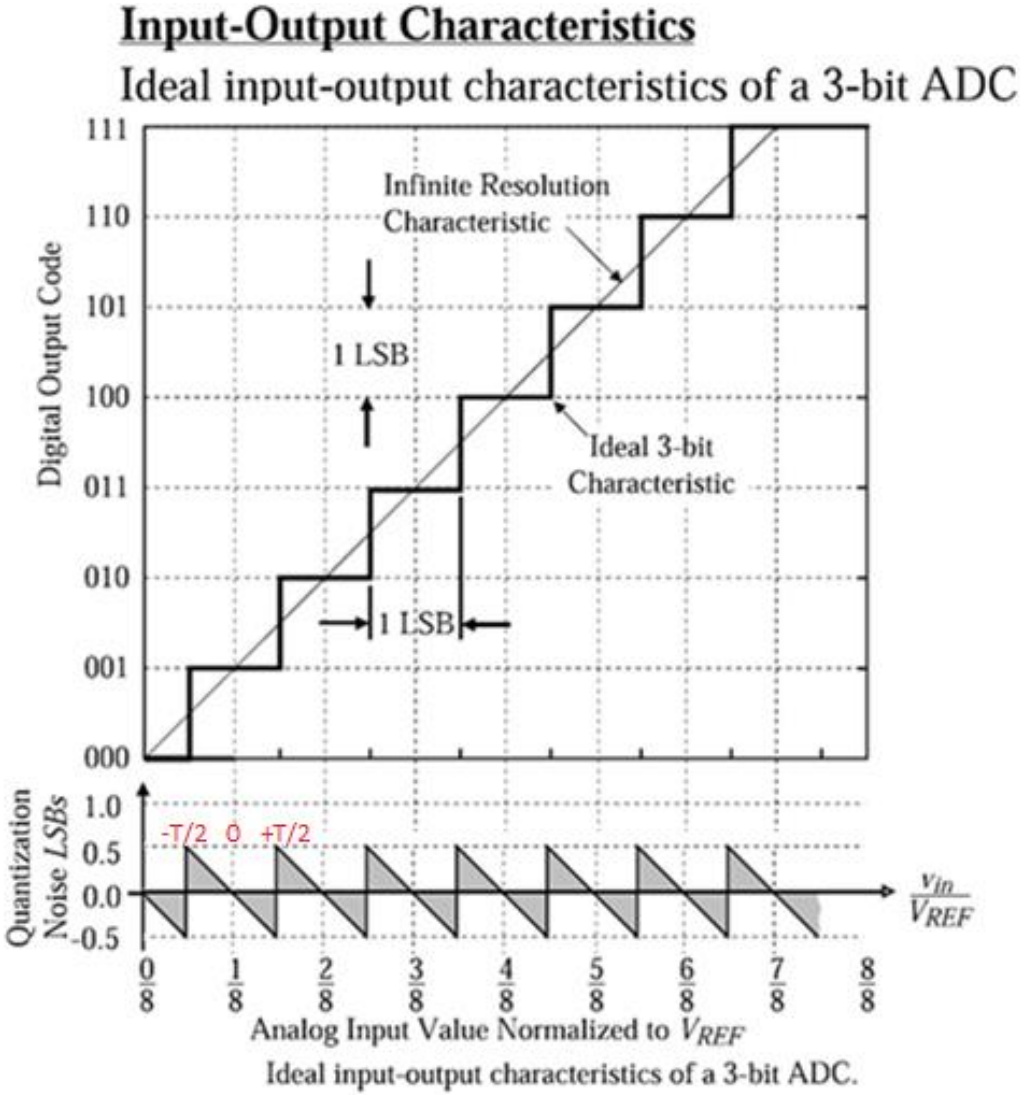
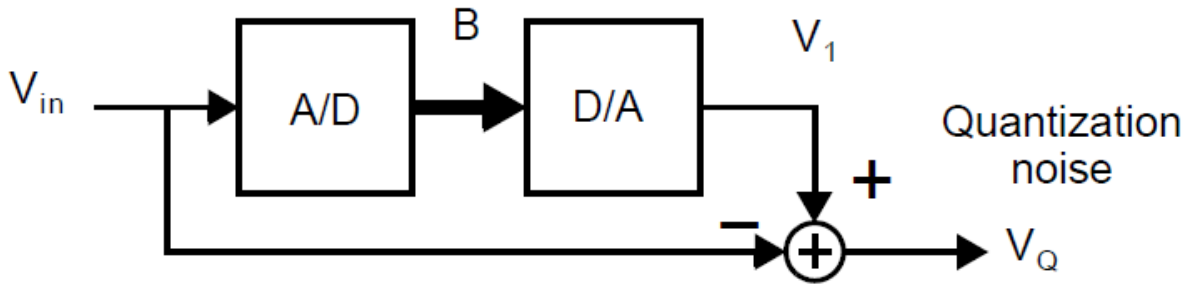
Analog to Digital (A/D) Converter

The operation of ADC is inverse of DAC function: Apply some sampled analog signal to generate the equivalent digital code.





- Quantization noise is the inherent uncertainty in digitizing an analog value with a finite resolution converter
- Quantization noise=Analog o/p of finite resolution characteristic- Analog o/p of infinite resolution characteristic

$$V_{Q(rms)} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_Q^2\, dt\right]^{1/2} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_{LSB}^2\left(\frac{-t}{T}\right)^2 dt\right]^{1/2}$$

$$= \left[\frac{V_{LSB}^2}{T^3}\left(\frac{t^3}{3}\Big|_{-T/2}^{T/2}\right)\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$

- *Resolution* of the ADC is the smallest analog change that distinguishable by an ADC.
- *Quantization Noise* is the $\pm 0.5 LSB$ uncertainty between the infinite resolution characteristic and the actual characteristic.
- *Offset Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic
- *Gain Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic measured at full-scale input. This difference is *proportional* to the analog input voltage.

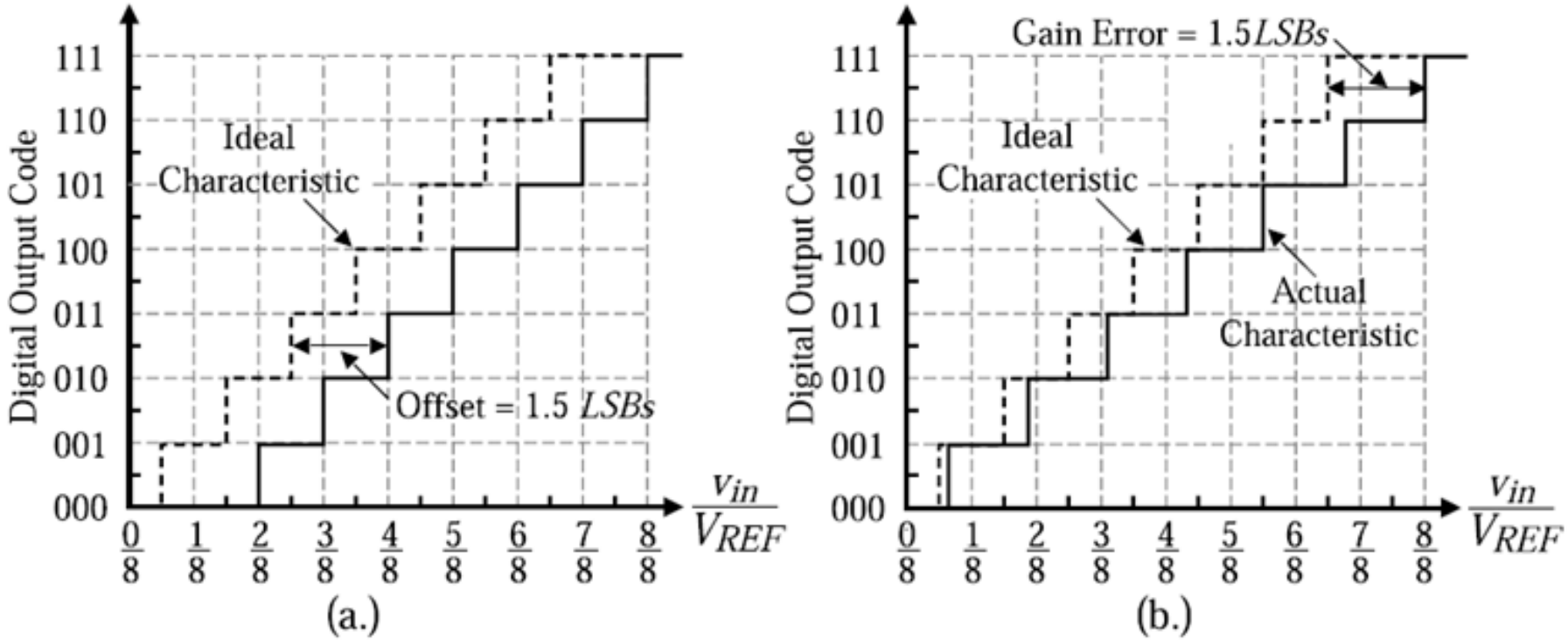


Figure 10.5-4 - (a.) Example of offset error for a 3-bit ADC. (b.) Example of gain error for a 3-bit ADC.

- *Dynamic Range* (*DR*) of a ADC is the ratio of the *FS*R to the smallest difference that can be resolved (i.e. an *LSB*)

$$DR = \frac{FSR}{LSB \text{ change}} = \frac{FSR}{(FSR/2^N)} = 2^N$$

or in terms of decibels

$$DR(\text{dB}) = 6.02N\,(\text{dB})$$

- *Signal-to-noise ratio* (*SNR*) for the ADC is the ratio of the full scale value to the *rms* value of the quantization noise.

$$rms(\text{quantization noise}) = \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N\sqrt{12}}$$

$$\therefore \quad SNR = \frac{v_{OUT}(rms)}{(FSR/\sqrt{12}\,2^N)}$$

- *Maximum SNR* (SNR_{max}) for a sinusoid is defined as

$$SNR_{max} = \frac{v_{OUT_{max}}(rms)}{(FSR/\sqrt{12}\,2^N)} = \frac{FSR/(2\sqrt{2})}{FSR/(\sqrt{12}\,2^N)} = \frac{\sqrt{6}\,2^N}{2}$$

or in terms of decibels

$$SNR_{max}(\text{dB}) = 20log_{10}\left(\frac{\sqrt{6}2^N}{2}\right) = 10\ log_{10}(6)+20\ log_{10}(2^N)-20\ log_{10}(2) = 1.76 + 6.02N\,\text{dB}$$

- *Effective number of bits (ENOB)* can be defined from the above as

$$ENOB = \frac{SNR_{Actual} - 1.76}{6.02}$$

where SNR_{Actual} is the actual *SNR* of the converter.

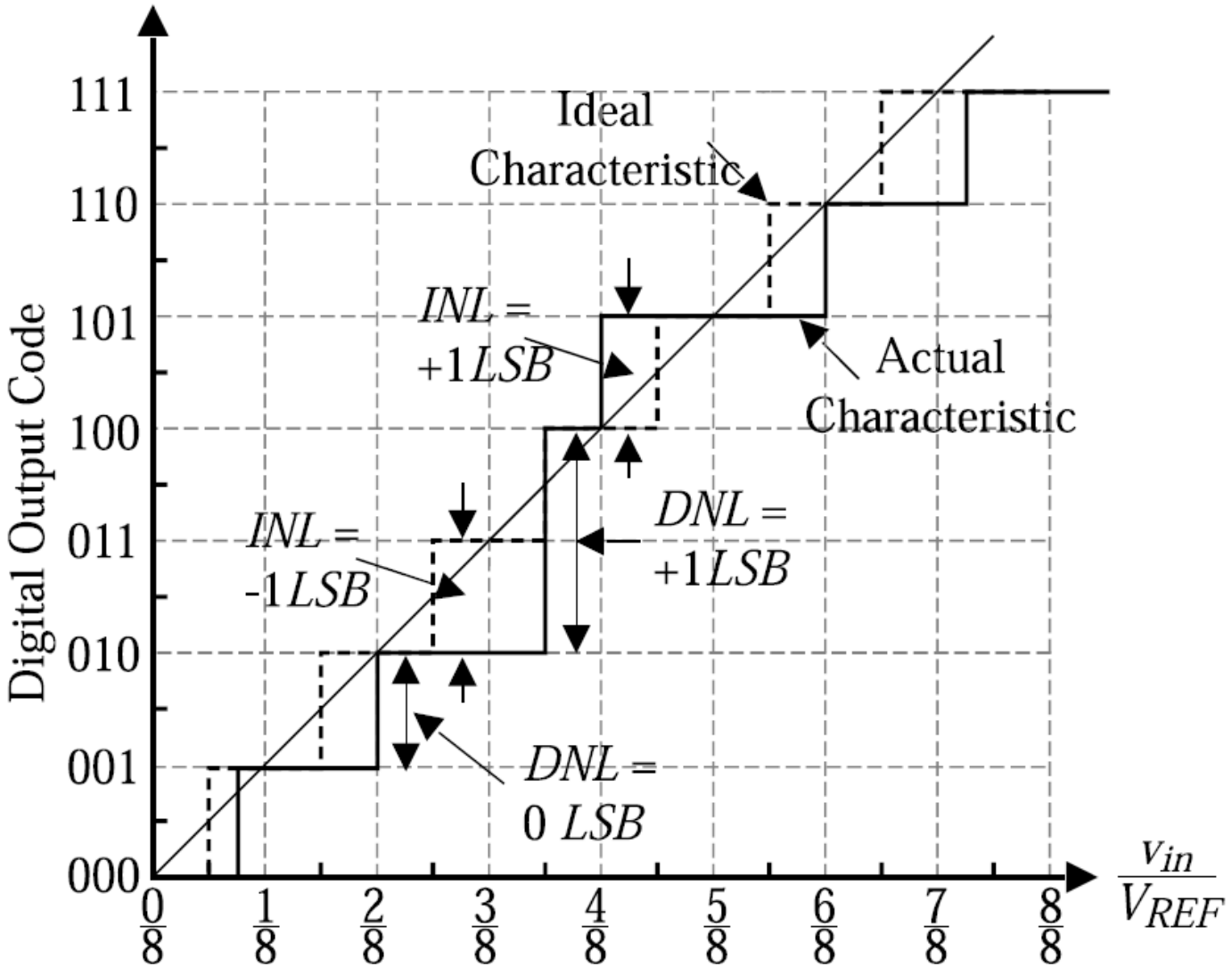
1. SNR_{max}(dB) provides the best possible SNR for an N-bit ADC.
2. However, actual SNR (i.e. SNR_{Actual})decreases from the SNR_{max} for a reduced signal level.
3. For example: in a 10 bit ADC, SNR_{max}=(60.2+1.76) dB=61.96 dB
   If the input signal becomes half (i.e. $0.5V_{REF}$), then
   $SNR_{Actual}=SNR_{max}-20\log 2=61.96-6.02=55.94$ dB
   ENOB=(55.94-1.76)/6.02=9

Integral and Differential Nonlinearity

The integral and differential nonlinearity of the ADC are referenced to the vertical (digital) axis of the transfer characteristic.

- *Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*)
- *Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical step (% or *LSB*).

Example of *INL* and *DNL*



Example of *INL* and *DNL* for a 3-bit ADC.) Fig.10.5-5

Note that the DNL and INL errors can be specified over some range of the analog input.

DYNAMIC CHARACTERISTICS OF ADCs

What are the Important Dynamic Characteristics for ADCs?

The dynamic characteristics of ADCs are influenced by:

- Comparators
  - Linear response
  - Slew response
- Sample-hold circuits
- Circuit parasitics
- Logic propagation delay

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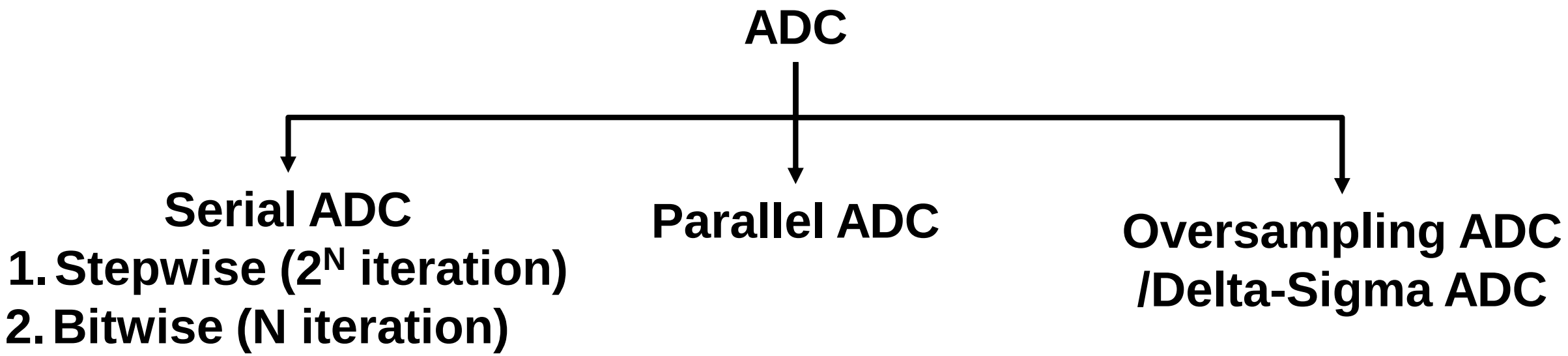
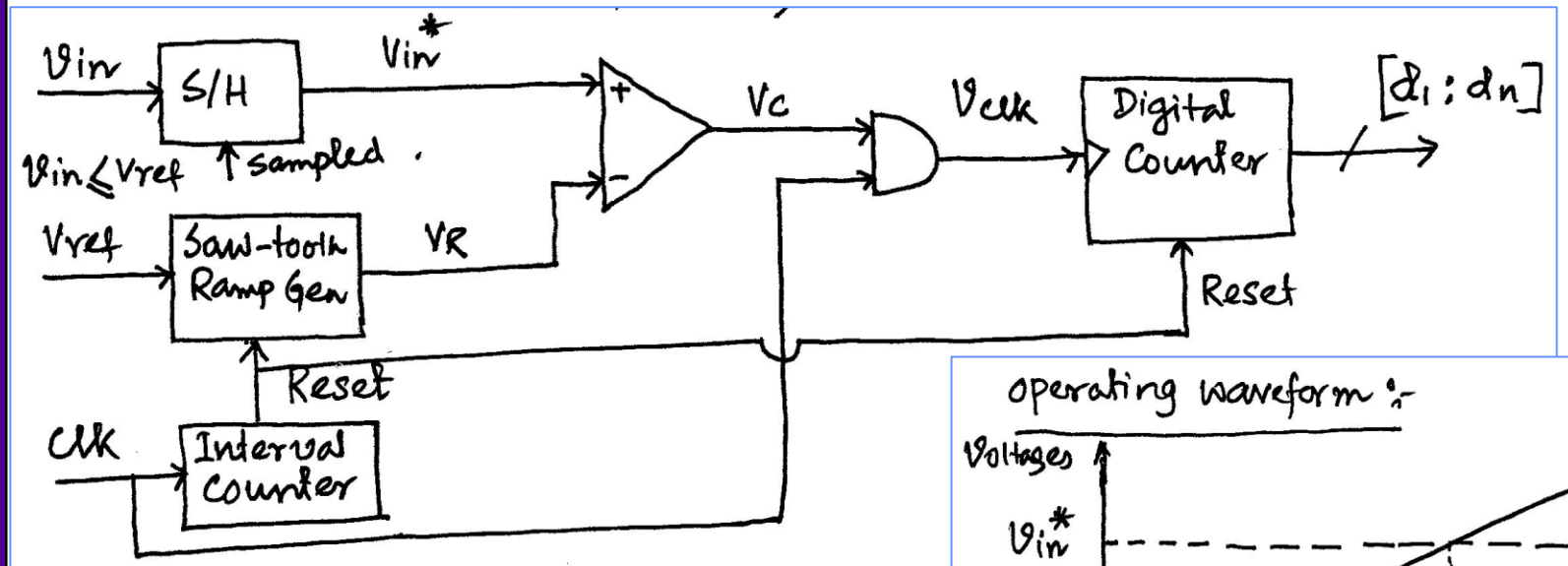
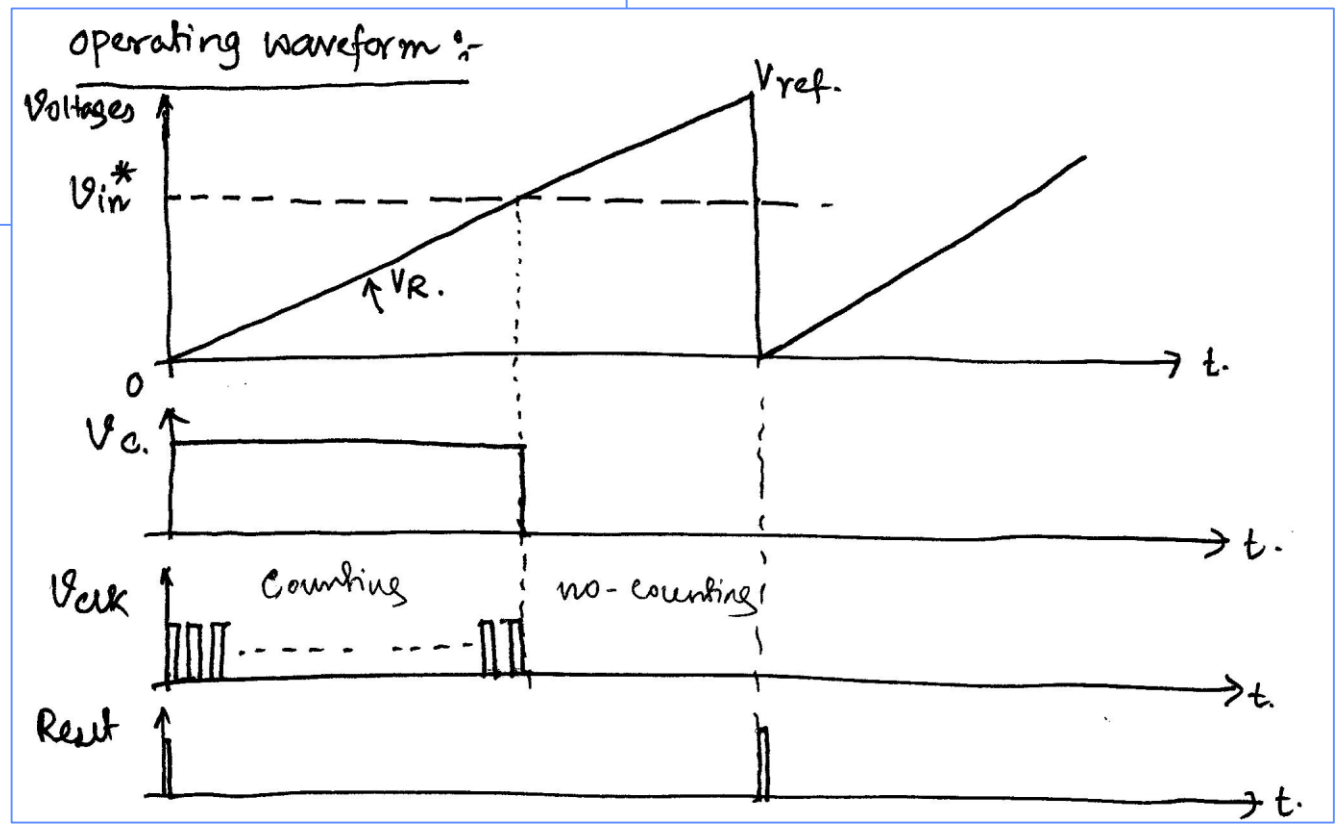

ADC
Serial ADC
1. Stepwise (2^N iteration)
2. Bitwise (N iteration)
Parallel ADC
Oversampling ADC
/Delta-Sigma ADC

Stepwise Serial ADC: Single Slope ADC





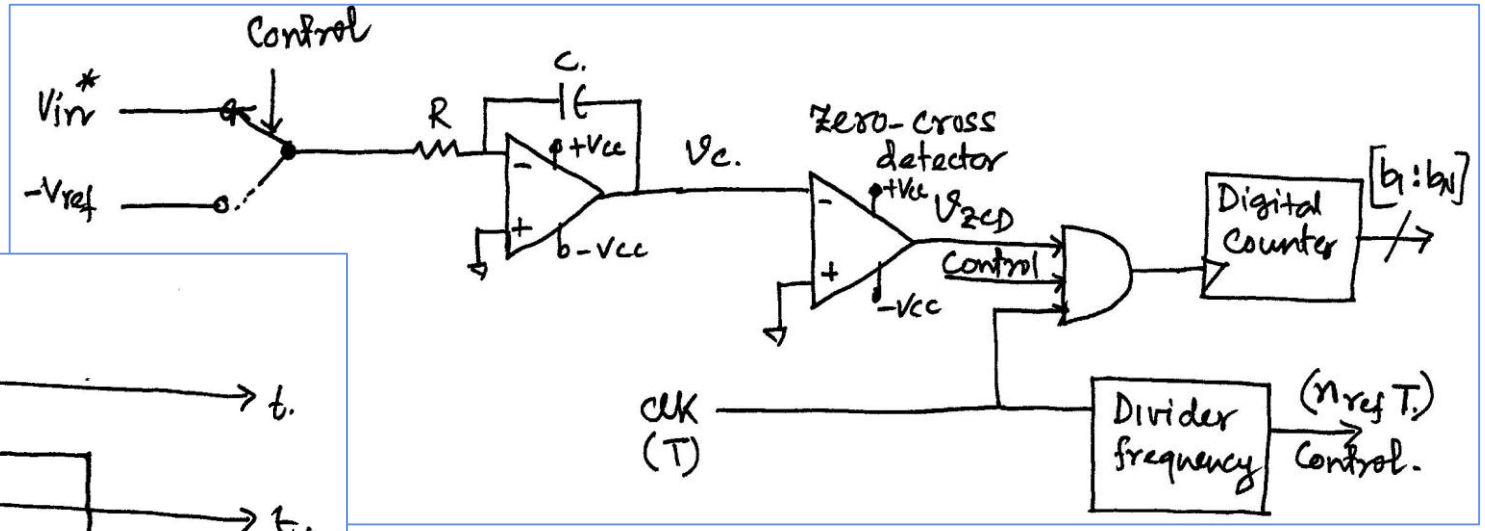
Advantage:

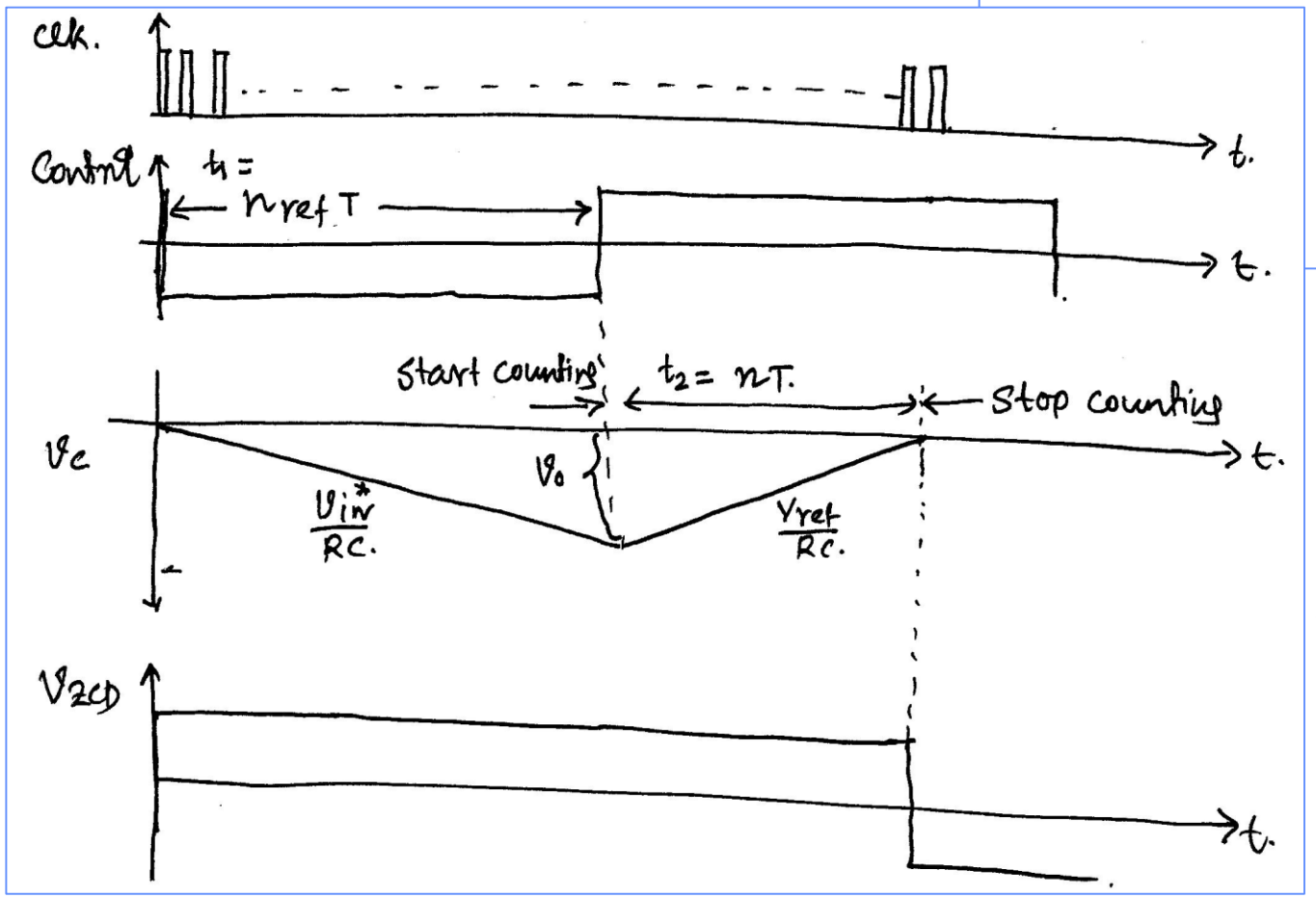
1. **Simple**

Disadvantages:

1. **Error in ramp rate leads to gain error in ADC**
2. **Comparator offset introduce error**
3. **High conversion time**
4. **Result drifts by CLK variation/jitter**

Stepwise Serial ADC: Dual Slope ADC





$$\frac{v_0}{t_1} = \frac{v_{in}^*}{RC}, \quad \frac{V_0}{t_2} = \frac{V_{ref}}{RC}$$

$$\frac{t_1 v_{in}^*}{RC} = \frac{t_2 V_{ref}}{RC}$$

$$n_{ref} T V_{in}^* = n T V_{ref}$$

$$n = \frac{n_{ref} V_{in}}{V_{ref}}$$

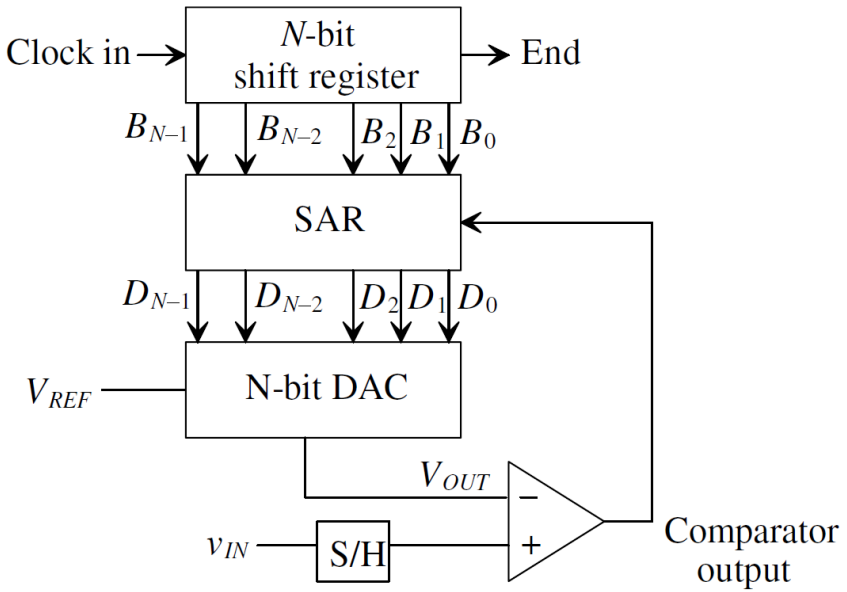
Advantages:

1. **Result does not drift by CLK variation.**
2. **Ramp rate variation does not introduce error.**

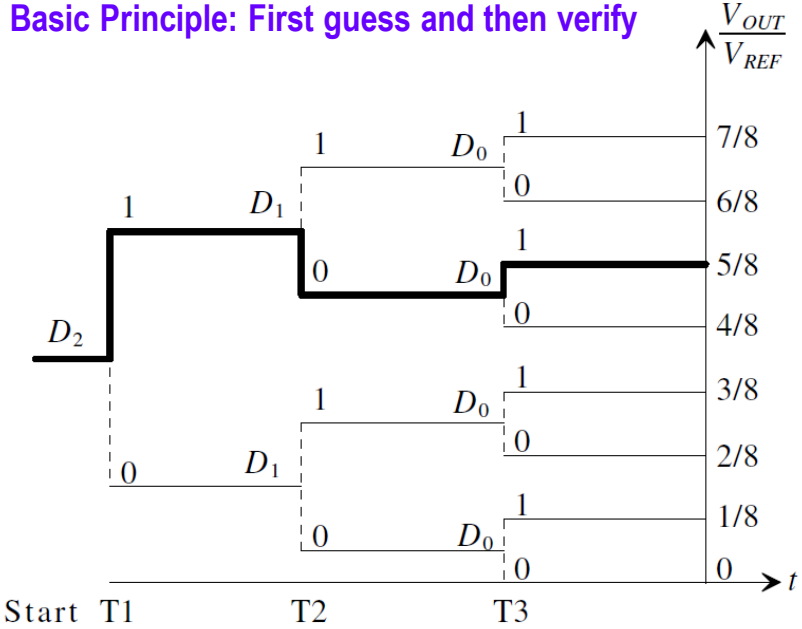
Disadvantage:

1. **Worst conversion time $2n_{ref}T$ for $V_{in}=V_{ref}$.**

Bitwise Serial ADC (Medium Speed): Successive Approximation ADC



Basic Principle: First guess and then verify



1. A 1 is applied to the input of the shift register. For each bit converted, the 1 is shifted to the right 1-bit position. $B_{N-1} = 1$ and B_{N-2} through $B_0 = 0$.
2. The MSB of the SAR, D_{N-1}, is initially set to 1, while the remaining bits, D_{N-2} through D_0, are set to 0.
3. Since the SAR output controls the DAC and the SAR output is 100...0, the DAC output will be set to $\frac{V_{REF}}{2}$.
4. Next, v_{IN} is compared to $\frac{V_{REF}}{2}$. If $\frac{V_{REF}}{2}$ is greater than v_{IN}, then the comparator output is a 0 and the comparator resets D_{N-1} to 0. If $\frac{V_{REF}}{2}$ is less than v_{IN}, then the comparator output is a 1 and the D_{N-1} remains a 1. D_{N-1} is the actual MSB of the final digital output code.
5. The 1 applied to the shift register is then shifted by one position so that $B_{N-2} = 1$, while the remaining bits are all 0.
6. D_{N-2} is set to a 1, D_{N-3} through D_0 remain 0, while D_{N-1} remains the value from the MSB conversion. The output of the DAC will now either equal $\frac{V_{REF}}{4}$ (if $D_{N-1} = 0$) or $\frac{3V_{REF}}{4}$ (if $D_{N-1} = 1$).
7. Next, v_{IN} is compared to the output of the DAC. If the DAC output is greater than v_{IN} then the comparator output drives D_{N-2} to 0. If the DAC output is less than v_{IN} then D_{N-2} remains a 1.
8. The process repeats until the output of the DAC converges to the value of v_{IN} within the resolution of the converter.

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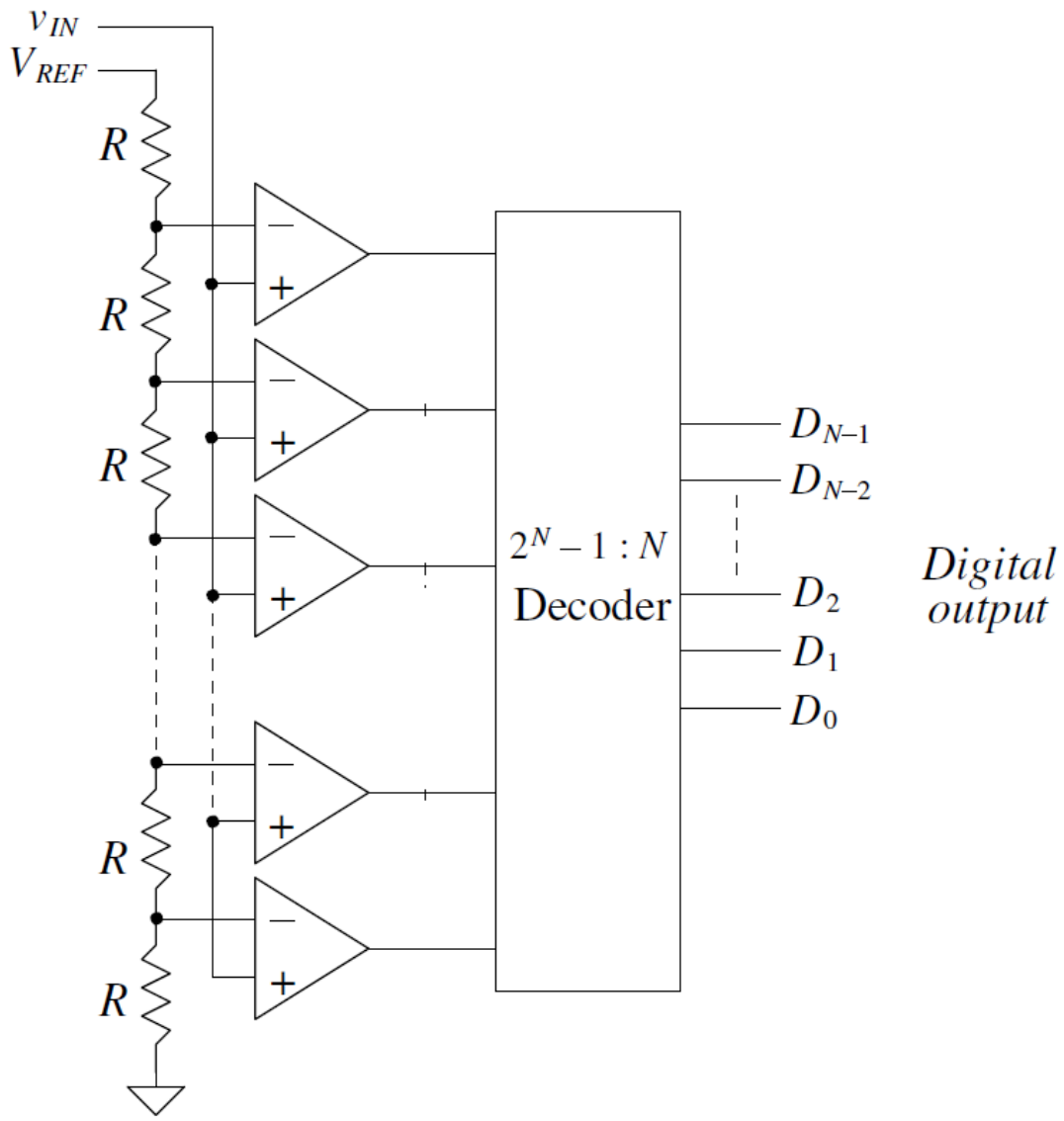
Parallel ADC (High Speed): Flash ADC

1. In many application, smaller conversion time is preferred.
2. In Flash ADC, it is one clock cycle having 2 phases.
   a) First phase: sampling and comparison
   b) Second phase: Decoder produce the equivalent digital word as output.
3. Advantage: Very fast.
4. Disadvantages:
   a) Requires 2^N equal resistors; occupies more area
   b) Requires (2^N-1) comparators; e.g., for N=6, 63 comparators are required; occupies more area and power.
   c) Low input bandwidth as the input is driving (2^N-1) comparators.
   d) Input CM of comparators differ, may have different delay.

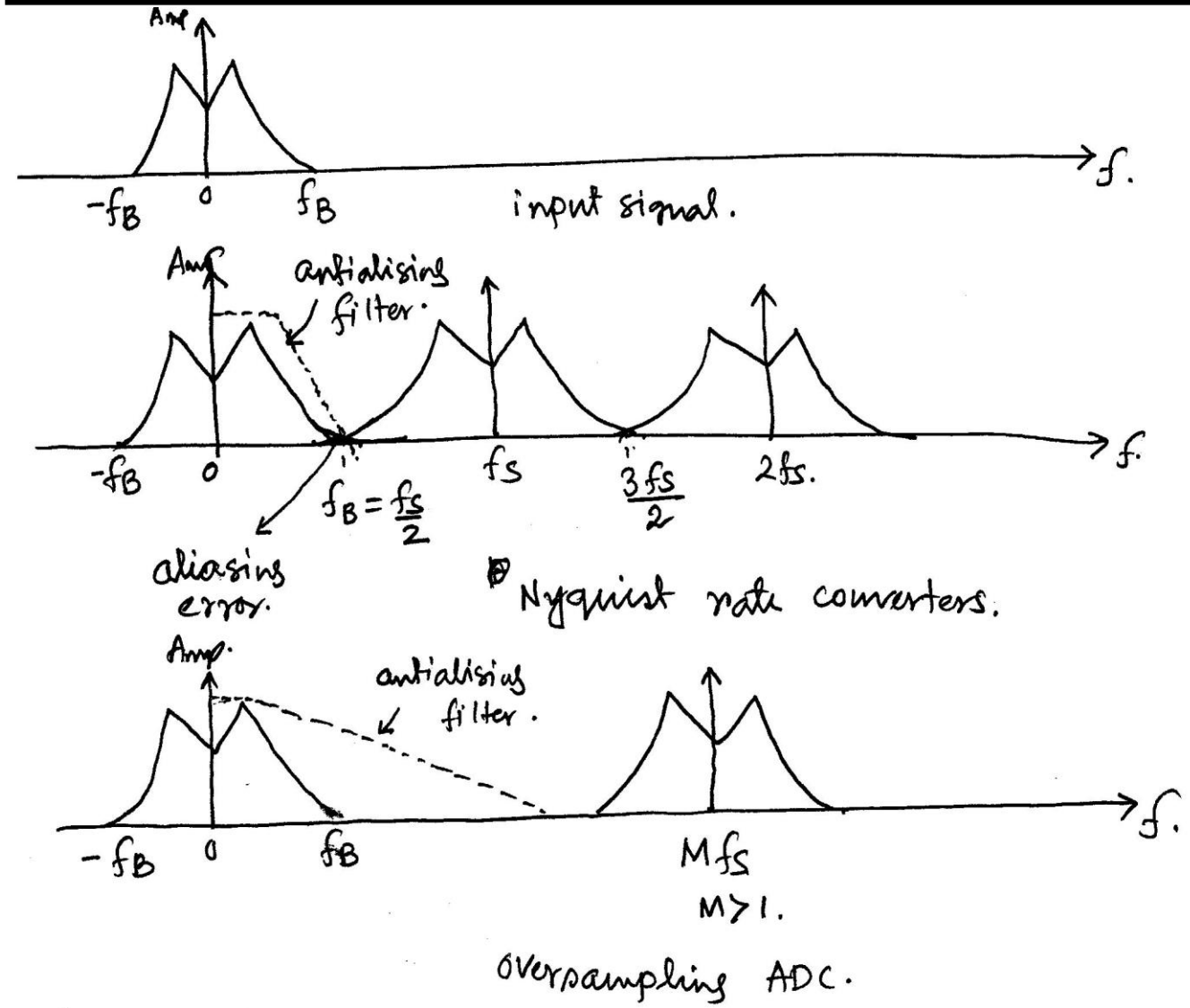


Oversampling ADC

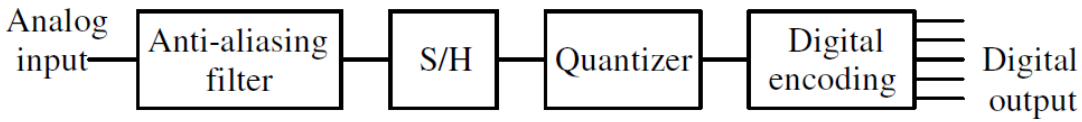
Two categories of ADCs depending on the rate of sampling.

1. Nyquist rate ADC where $f_S = 2f_B$ where f_B is the bandwidth of the signal and f_S is the sampling rate.
   a) Very fast, resolution is limited to 10-12 bits due to limited matching
2. Oversampling ADC where $f_S > 2f_B$
   a) Different class of ADCs and does not require precise component matching.
   b) Digital signal processing techniques are used in place of precise analog components.
   c) The accuracy of the converter does not depend on the component matching, precise sample-and-hold circuitry, or trimming, and only a small amount of analog circuitry is required. Switched-capacitor implementations are easily achieved, and, as a result of the high sampling rate, only simplistic anti-aliasing circuitry needs to be used.
   d) However, because of the time required to sample the input signal, the throughput is considerably less than the Nyquist rate ADCs.
   e) It provides much higher resolution than the Nyquist rate converters.
   f) Two key principle used in oversampling ADCs: oversampling and noise shaping

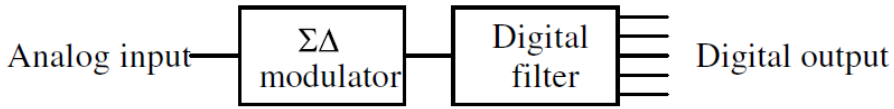
Difference between Nyquist rate and oversampling ADCs



1. **Antialiasing filter requirement in oversampling ADC is much more relaxed than Nyquist rate ADC.**
2. **No dedicated S/H circuit is required in oversampling ADC**
3. **Quantization is performed in the modulator and encoding takes place in digital filter.**



(a)

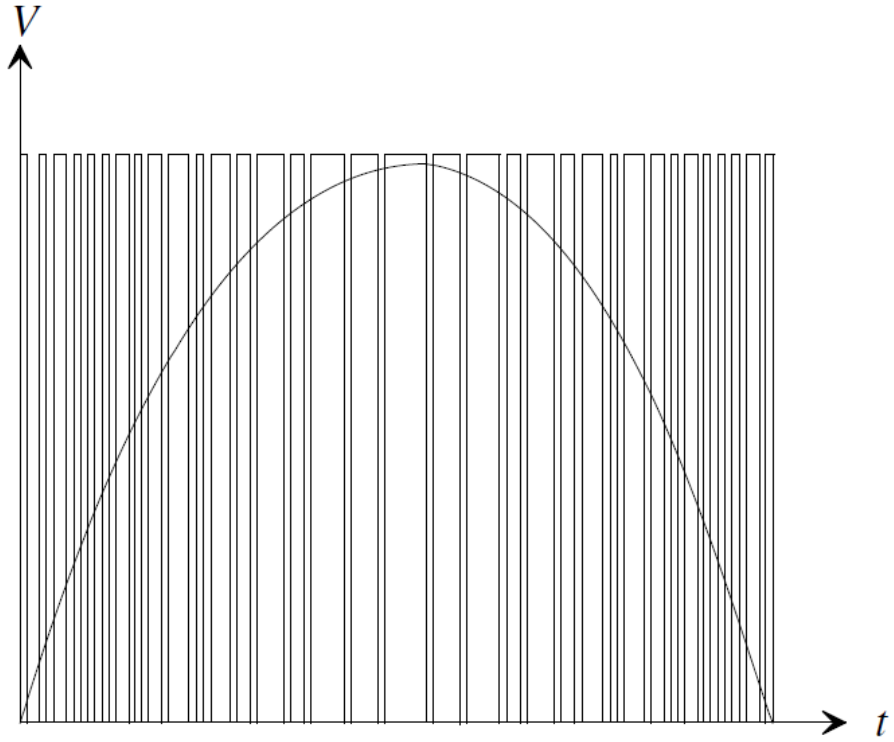


(b)

Typical block diagram for (a) Nyquist rate converters and (b) oversampling ADCs.

ΣΔ Modulator

1. The ΣΔ modulator provides the quantization in the form of a pulse-density modulated signal.
2. The density of the pulses represents the average value of the signal over a specific period. For the peak of the sine wave, most of the pulses are high. As the sine wave decreases in value, the pulses become distributed between high and low according to the sine wave value.
3. If the frequency of the sine wave represented the highest frequency component of the input signal, a Nyquist rate converter would take only two samples.
4. The oversampling converter, however, may take hundreds of samples over the same period to produce this pulse-density signal.
5. Digital signal processing is then used, which has two purposes:
   a) To filter any out-of-band quantization noise and to attenuate any spurious out-of-band signals.
   b) The output of the filter is then down-sampled to the Nyquist rate so that the resulting output of the ADC is the digital data.



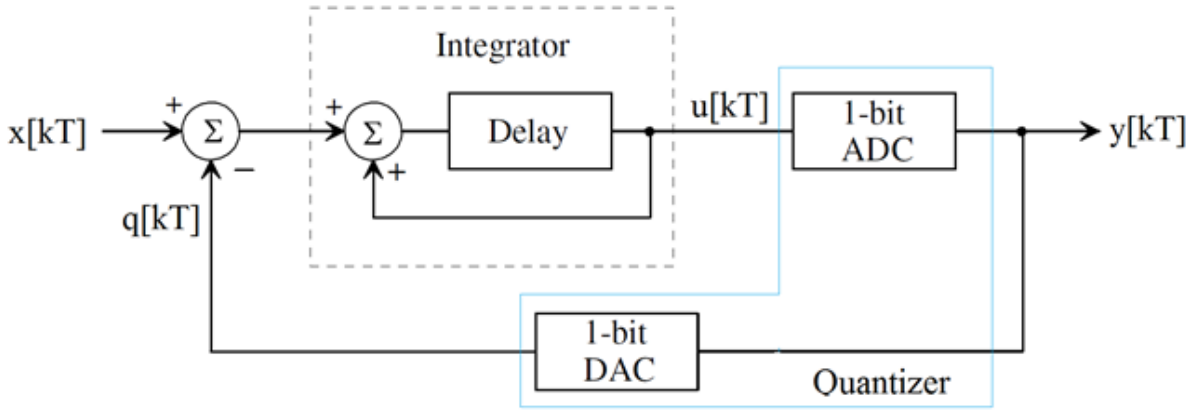
Pulse-density output from a sigma-delta modulator for a sine wave input.

The first order ΣΔ Modulator

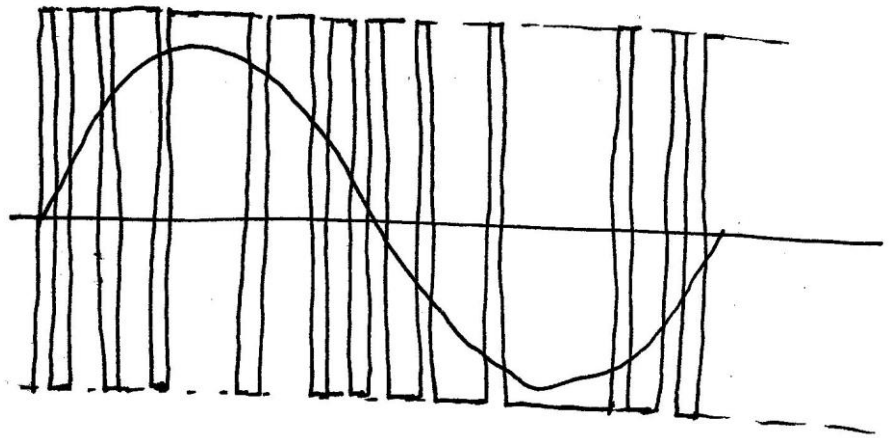
1. Only one integrator is used, hence first order.
2. 1-bit ADC is nothing but a comparator.
3. 1-bit DAC uses comparator output y[kT] to determine if $+V_{ref}$ or $-V_{ref}$ is summed with input x[kT]
4. If u[kT] is positive, y[kT]=High, q[kT]=$+V_{ref}$ and u[kT] moves in negative direction.
5. As u[kT] becomes negative, y[kT]=Low, q[kT]=$-V_{ref}$ and u[kT] moves to positive direction.
6. Integrator accumulates the error between x[kT] and q[kT] and negative feedback tries to make integrator's output zero.
7. Local average of x[kT] at a particular instant should be equal to the local average of the quantizer output.
8. This produces a pulse density modulated signal for a sine wave.

Try yourself!

$$\frac{Z^{-1}}{1-Z^{-1}}$$



A first-order sigma-delta modulator.



EE60032: Analog Signal Processing

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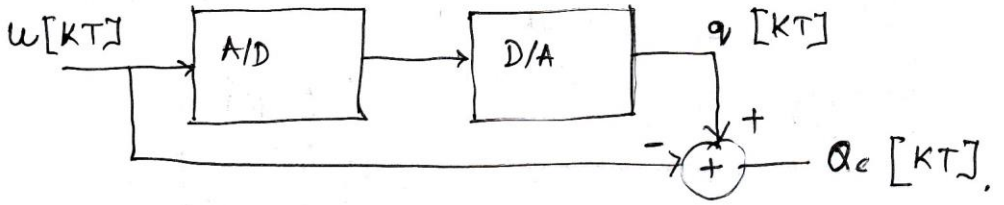
The first order ΣΔ Modulator

$u[KT] = x[KT-T] - q[KT-T] + u[KT-T]$

ADC introduces quantization noise.



$Qe[KT] = q[KT] - u[KT]$

Then, $q[KT] = Qe[KT] + x[KT-T] - q[KT-T] + u[KT-T]$

1 bit D/A has the following char.

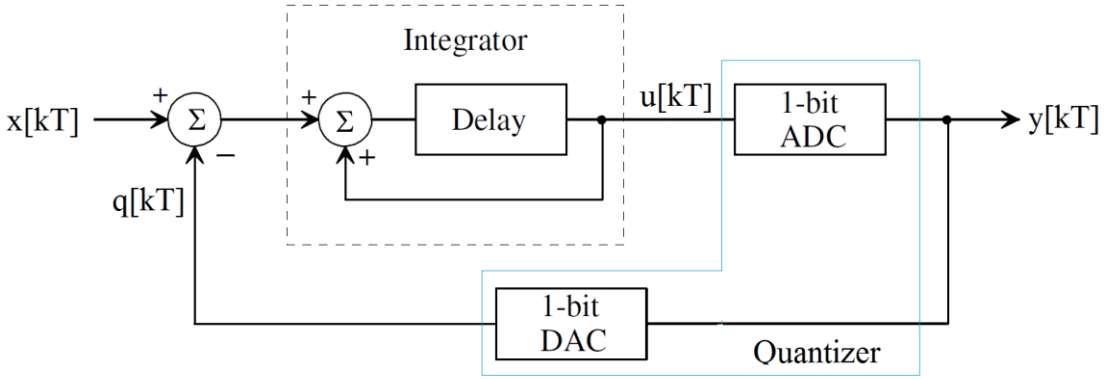
If $y[KT] = Low$, $q[KT] = -V_{ref}$ $\quad y[KT] = Low = -V_{ref}$.

$y[KT] = High$ $\quad q[KT] = +V_{ref}$ $\quad y[KT] = High = +V_{ref}$.

$y[KT] = q[KT]$

Then $y[KT] = Qe[KT] + x[KT-T] - Qe[KT-T]$

$= x[KT-T] + Qe[KT] - Qe[KT-T]$



A first-order sigma-delta modulator.

Here, quantization noise is getting reduced by previous value. That is the real power of ΣΔ Modulator

Frequency domain analysis of the first order ΣΔ Modulator

$$Y(s) = Q_e(s) + \frac{1}{s}\left[X(s) - Y(s)\right]$$

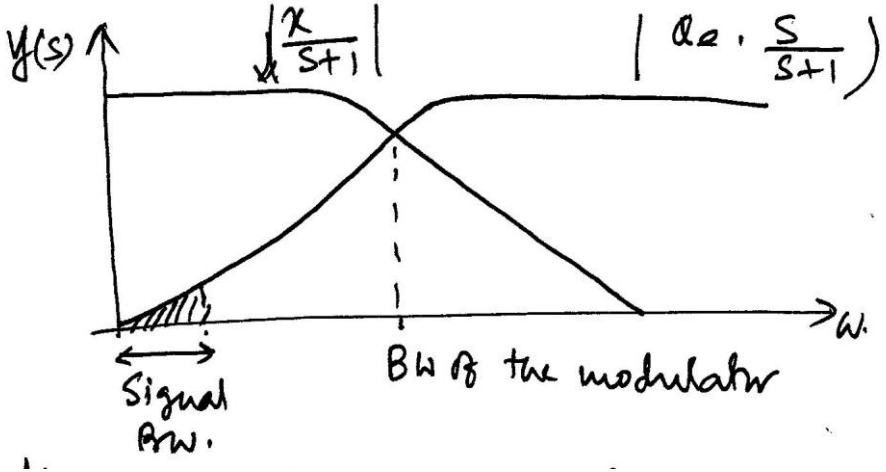
$$\text{or, } Y(s)\left[1 + \frac{1}{s}\right] = Q_e(s) + \frac{1}{s}X(s)$$

$$\text{or } Y(s) = \frac{Q_e(s)\,s}{(s+1)} + \frac{X(s)}{(s+1)}$$

$$= Q_e(s)\frac{s}{(s+1)} + X(s)\cdot\frac{1}{s+1}$$

$\frac{Y(s)}{X(s)}$ is a low pass filter.

$\frac{Y(s)}{Q_e(s)}$ is a high pass filter.

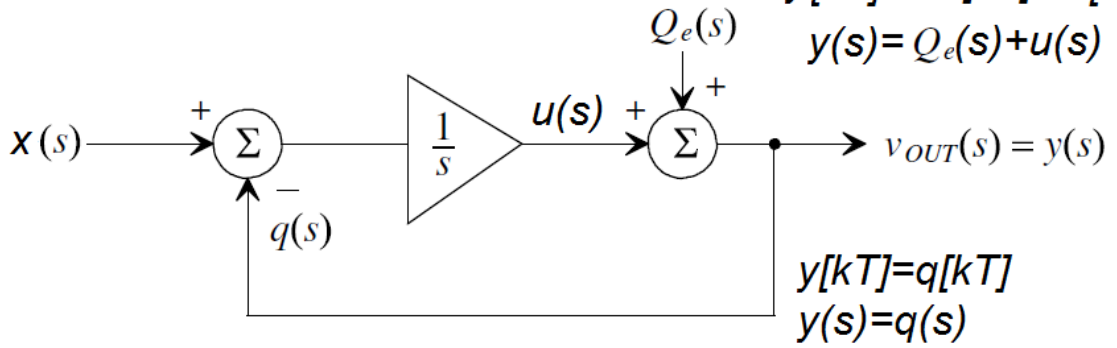


$Q_e[kT] = q[kT] - u[kT]$

$q[kT] = Q_e[kT] + u[kT]$

$y[kT] = Q_e[kT] + u[kT]$

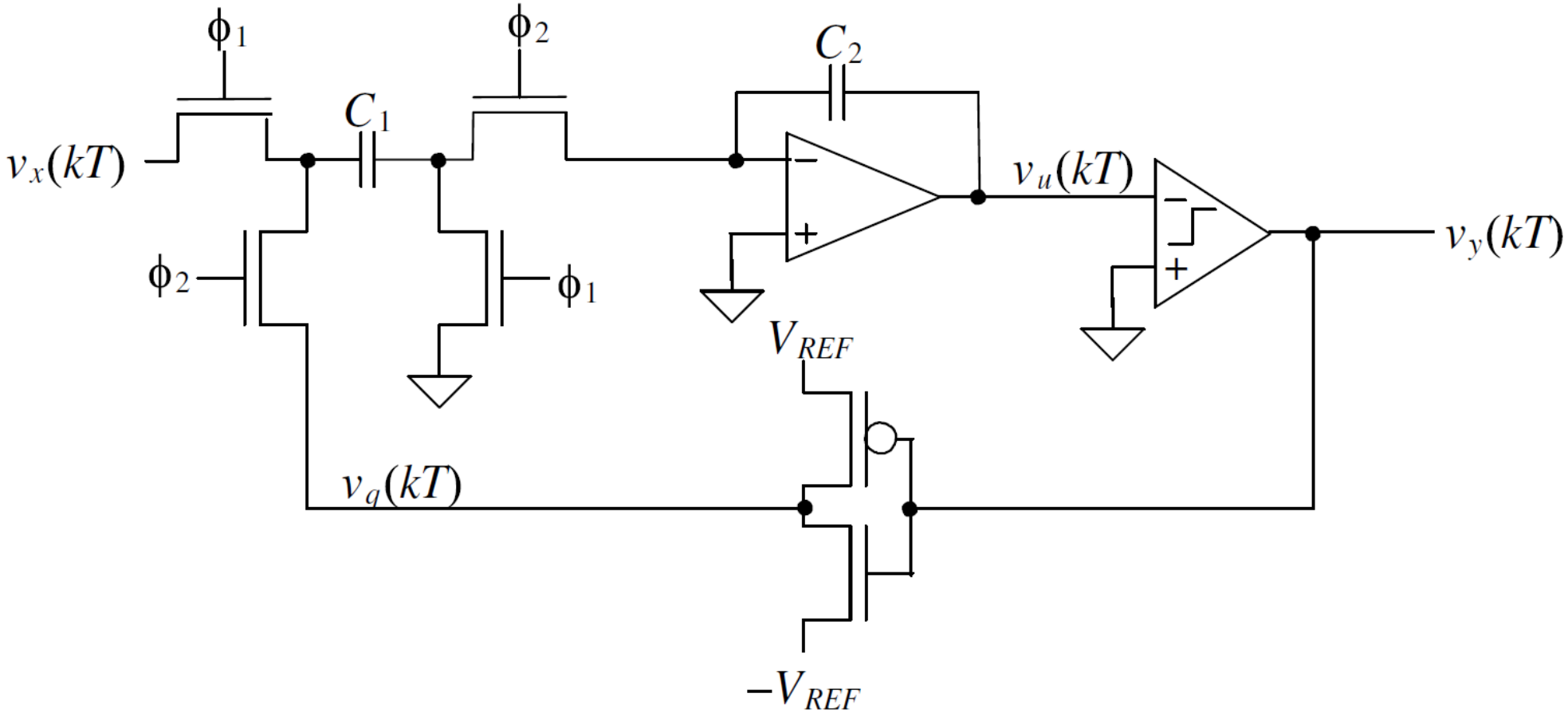
$y(s) = Q_e(s) + u(s)$



A frequency domain model for the first-order sigma-delta modulator.

1. Quantization noise is pushed to higher frequency: noise shaping
2. Low pass filtering is then performed in digital filter to remove out-of-band quantization noise.
3. Then, we down-sampled to yield final high resolution output.

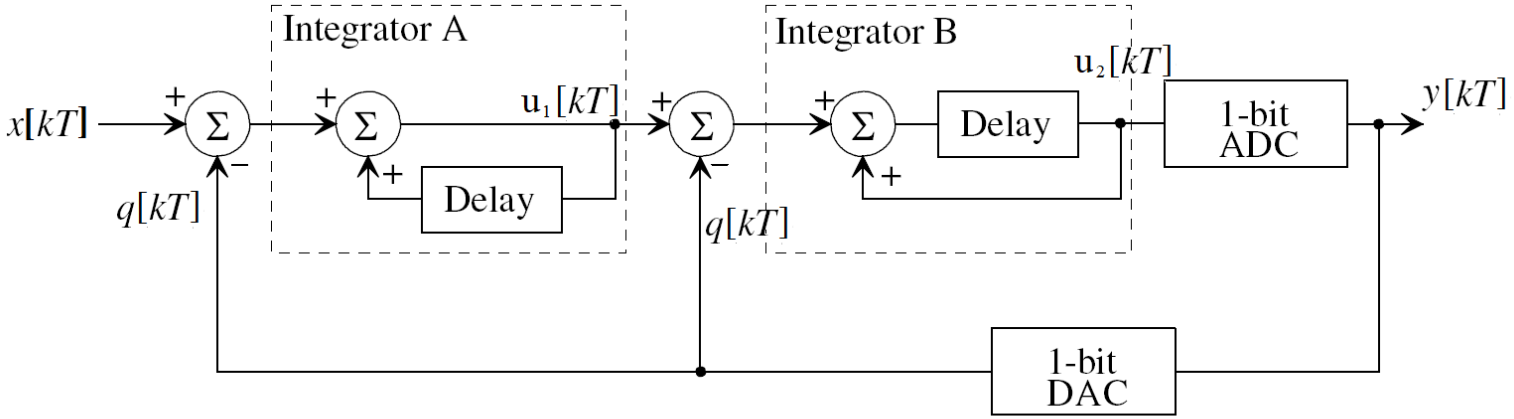
Implementation of the first order ΣΔ Modulator



Implementation of a first-order sigma-delta modulator using a switched capacitor integrator.

Second order ΣΔ Modulator

1. **Higher order ΣΔ Modulator use more no. of integrators and provide a greater amount of noise shaping**



A second-order, sigma-delta modulator.

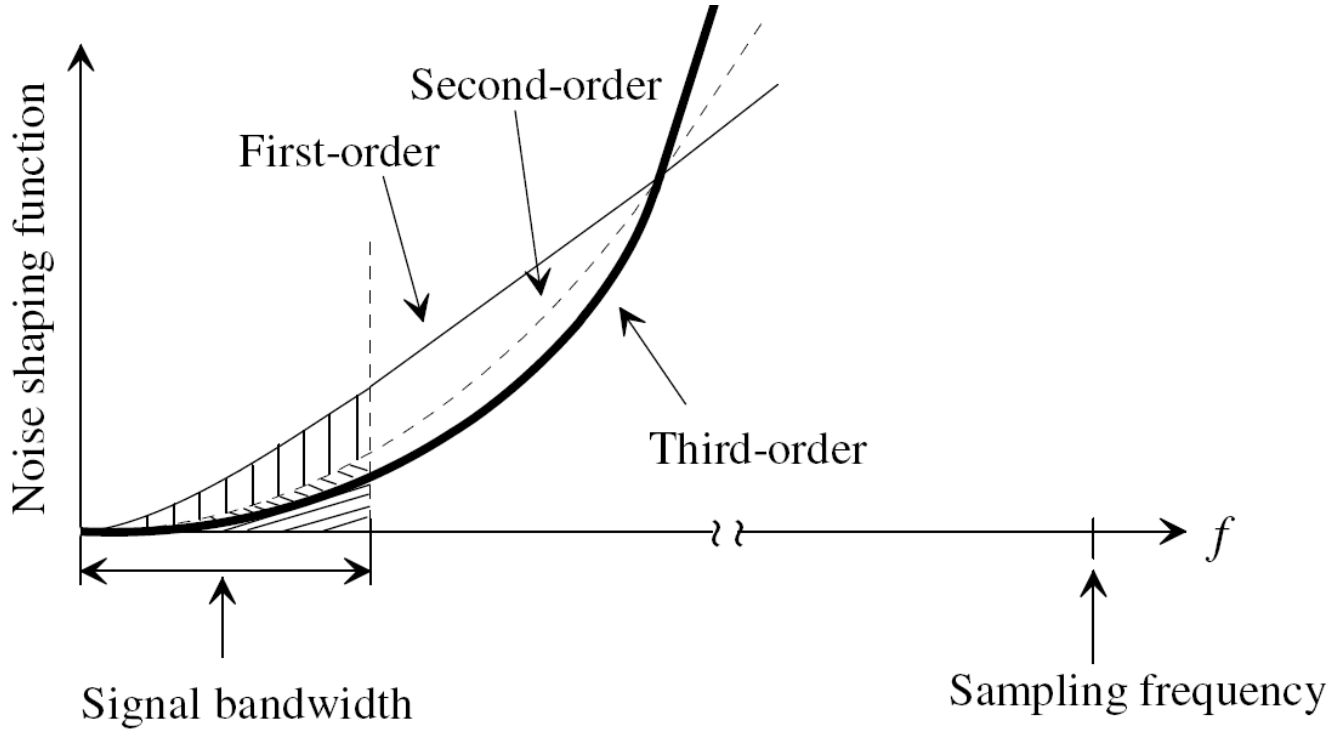
Try Yourself!

$y[kT]=x[kT-T]+Q_e[kT]-Q_e[kT-T]-\{Q_e[kT-T]-Q_e[kT-2T]\}$

$y[kT]=x[kT-T]+Q_e[kT]-2Q_e[kT-T]+Q_e[kT-2T]$

Second order ΣΔ Modulator

1. As the order increases, more of the noise is pushed out into the higher frequencies, thus decreasing the noise in the signal bandwidth.
2. The **ΣΔ** modulators do not attenuate noise at all. In fact, they add quantization noise that is very large at high frequencies.
3. The **ΣΔ** modulator should not be construed as a filtering circuit.



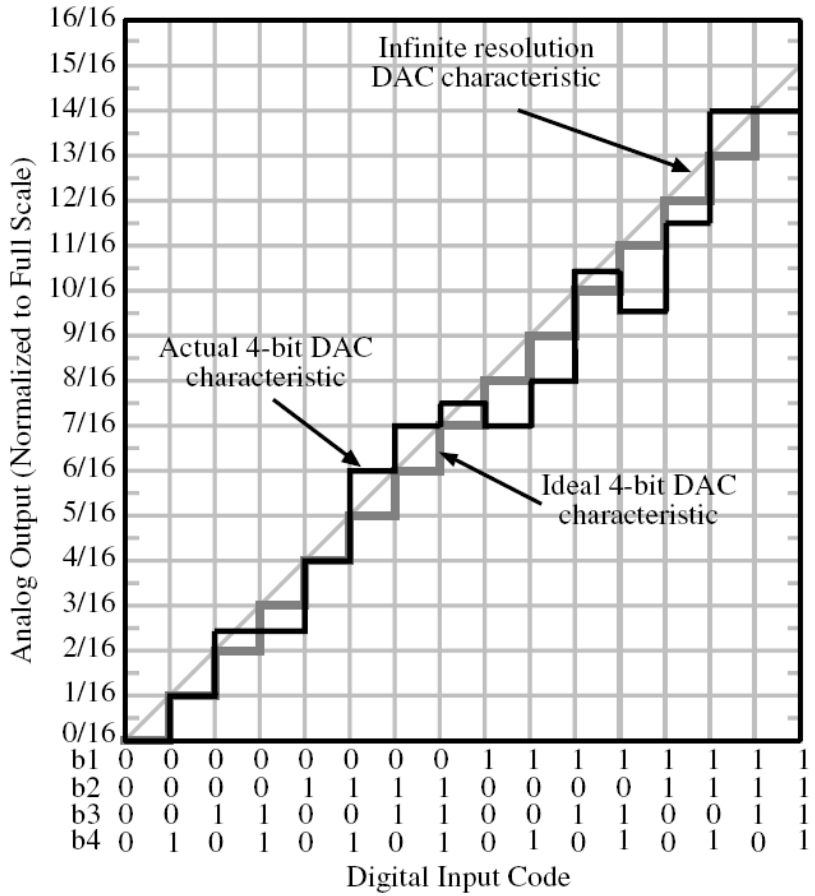
Noise shaping comparison of a first-, second- and third-order modulator.

Note: A high-order ΣΔ modulator with many integrators. However, as with any system employing feedback, stability becomes a critical issue.

Try yourself!

1. Find the resolution for a DAC if the output voltage is desired to change in 1 mV increments while using a reference voltage of 5V.

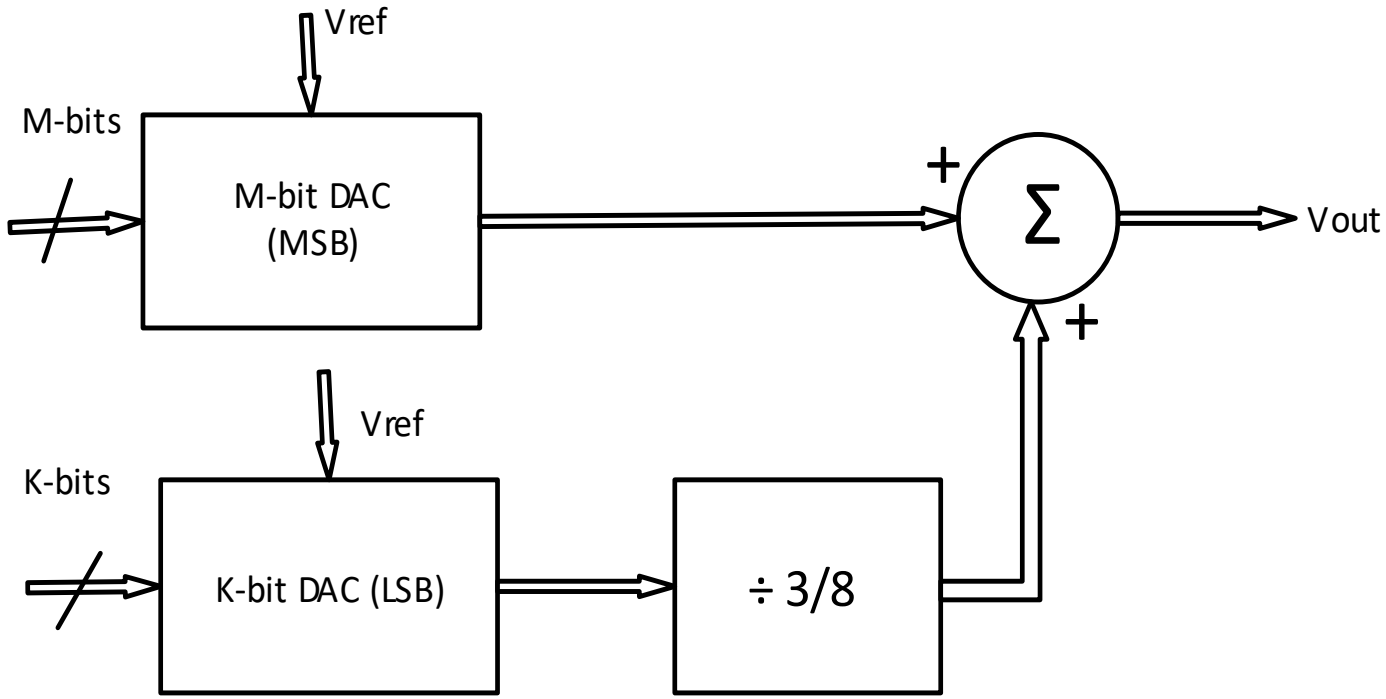
2. From any non-ideal characteristics of the DAC converter, find out INL and DNL in terms of LSBs.



Try yourself!

3. Draw a serial DAC circuit. Show the conversion process with operating waveform when a digital word $b_1b_2b_3b_4$=1010 is applied to the serial DAC. Assume b_4 is LSB and b_1 is MSB. No need to describe the operation.

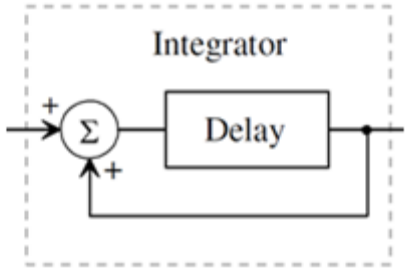
4. Assume M=2 and K=2, find out the transfer characteristic of this DAC if the scaling factor of the LSB sub-DAC is 3/8 instead of 1/4. Assume V_{ref}=1 V. What is the ±INL and ±DNL for this DAC? Is this DAC monotonic?



Try yourself!

5. An 8-bit ADC has a reference voltage V_{ref}=4V. Find the RMS value of the quantization noise. Also find SNR of the ADC for full scale sine wave input and half scale sine wave input.

6. Prove that the following block gives you an integrator operation



7. Draw a second-order Σ-Δ modulator and derive the expression of its output.

Submission deadline: 10th of November midnight