Analog Signal Processing (EE60032),

Department of Electrical Engineering, Indian Institute of Technology, Kharagpur

Tutorial Module 1: Signal Processing Using Operational Amplifier

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- **Amplifier with different non-idealities**

1. Design an inverting amplifier for a nominal gain of 4, a gain error of 0.1% and an input impedance of 10 kΩ. [Ans. $R_2 = 40\ \text{k}\Omega$, $A_{ol} = 5005$]

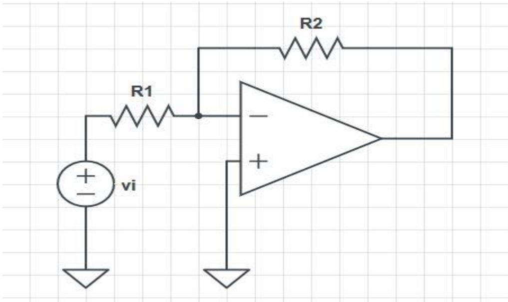

Figure 1

2. Design an inverting amplifier as shown in the figure 2 to get a dc gain of -10 and an input impedance of 10 MΩ. Calculate R_t , R_s and R_1. [Ans. $R_1 = 10\ \text{M}\Omega$, $R_t = 47\ \text{k}\Omega$, $R_s = 22\ \Omega$]

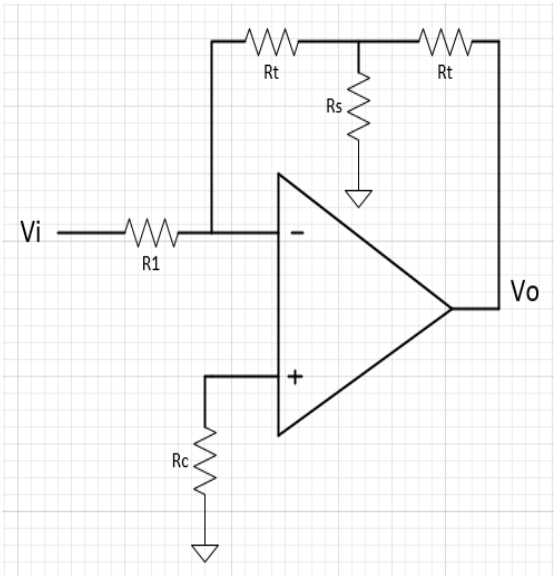

Figure 2

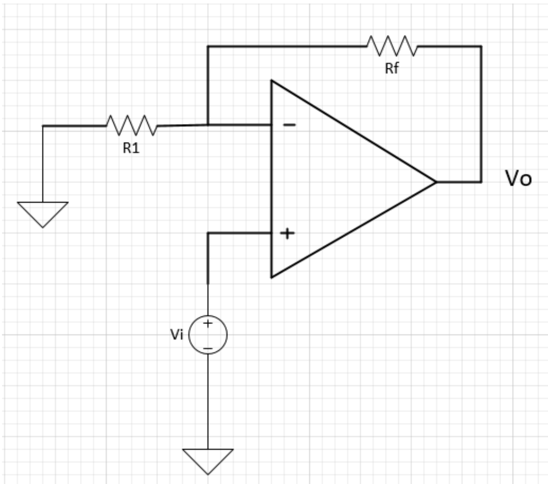

Figure 3

3. For the non-inverting amplifier as shown in the figure 3, R_1= 1 KΩ, R_f= 10 KΩ.
   a) Calculate the maximum output offset voltage due to V_{ios} and I_B. Assume the op-amp has V_{ios}= 10 mV, I_B= 300 nA and I_{os}= 50 nA.
   b) Calculate the value of R_{comp} needed to reduce the effect of I_B.
   c) Calculate the maximum output offset voltage if R_{comp} as calculated in (b) is connected in the circuit.

[Ans. a) 113 mV, b) 0.9 kΩ, c) 110.5 mV]

4. In an inverting amplifier R_1= 100 KΩ, R_f= 10 MΩ. [Ans. a) 606 mV. b) 6 V]
   a) Calculate maximum output offset voltage caused by input offset voltage V_{ios};
   b) Calculate maximum output offset voltage caused by input bias current I_B;
   Where V_{ios}= 6 mV and I_B= 500 nA.

- **Adder/Subtractor:**

5. Design a circuit which can generate an output voltage $v_o=-2(3v_1+4v_2+2v_3)$, where v_1, v_2 and v_3 are the input voltages.
6. Design an adder circuit using op-amps to get $v_o= - (0.1v_1+v_2+10v_3)$, where v_1, v_2 and v_3 are the inputs.
7. Find V_o in figure 4. [Ans. 6.568 V]

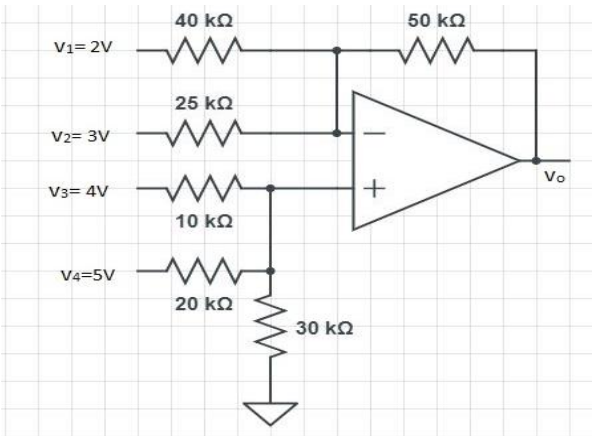

Figure 4

8. Show that $v_o= a_1v_1+a_2v_2+a_3v_3$. Find a_1, a_2 and a_3. Find the value of v_o if
   i) R_4 is shorted.
   ii) R_4 is removed.
   iii) R_1 is shorted.

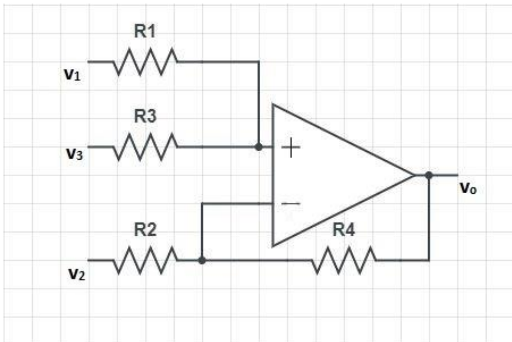

Figure 5

- **Op-amp circuit analysis:**

9. For the instrumentation amplifier shown in the figure 6 below, verify that $v_o = (1+R_2/R_1+2R_2/R)(v_2-v_1)$.

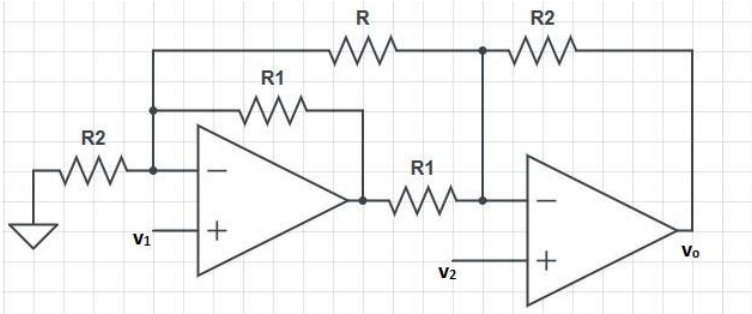

Figure 6

10. Calculate V_o for the circuit shown in the figure 7 below for V_1=5V and V_2= 2V. [Ans. 3V]

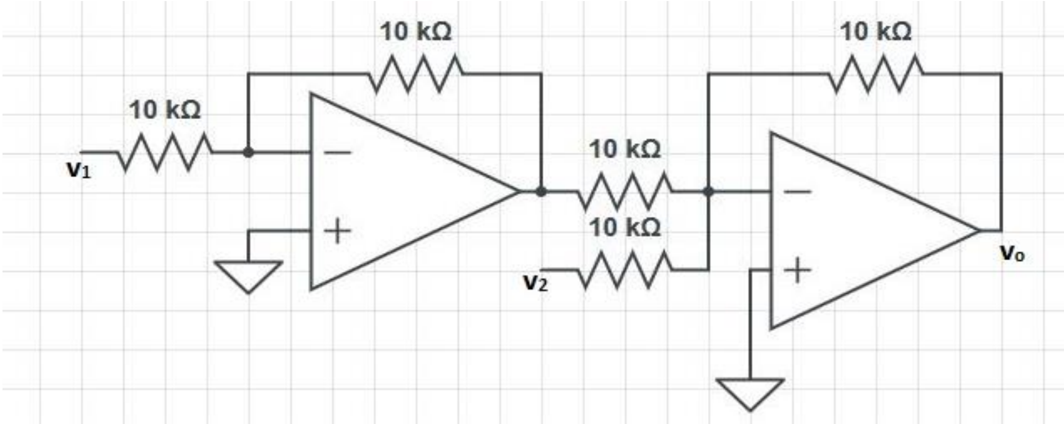

Figure 7

11. Compared with the classical triple op-amp, below in figure 8 uses fewer resistances. The wiper is nominally positioned halfway to maximize the CMRR. Show that $v_o = (1+2R_2/R_1)(v_2-v_1)$.

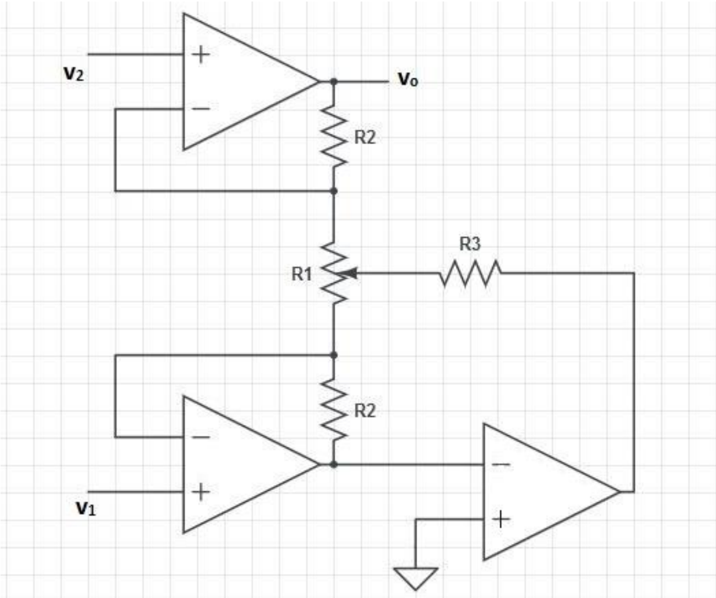

Figure 8

12. Show that $v_o = 2(1+R/R_G)(v_2-v_1)$ in figure 9.

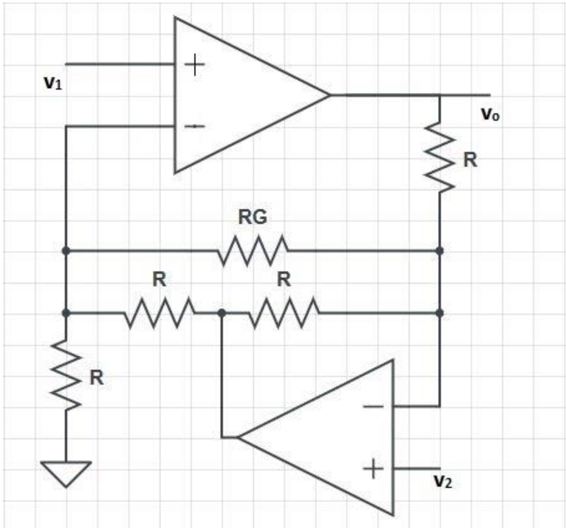

Figure 9

13. The circuit in figure 10 can be used to control the input resistance of the inverting amplifier based on OA_1.
    a) Show that $R_i = R_1/(1 - R_1/R_3)$.
    b) Specify resistances suitable for achieving $A = -10\ V/V$ with $R_i = \infty$.

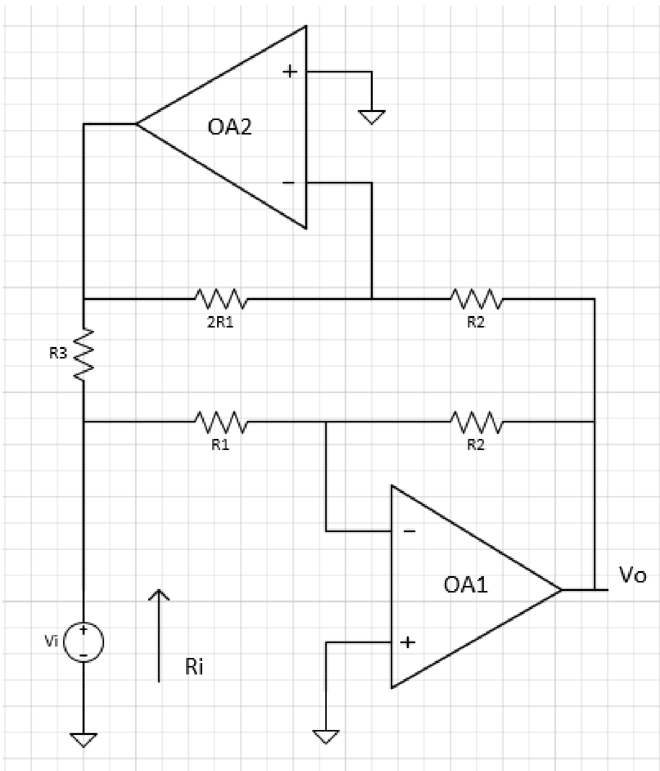

Figure 10

14. In the series-series circuit in figure 11, $A = 10^4\ V/V$, R_1=1 KΩ, R_2=2 KΩ and R_3=3 KΩ. Find a expression for $I_0 = A_g V_I - V_L/R_0$. What is the value of A_g and R_0.

[Ans. A_g =2×10^{-3}, R_0 =5×10^{6}]

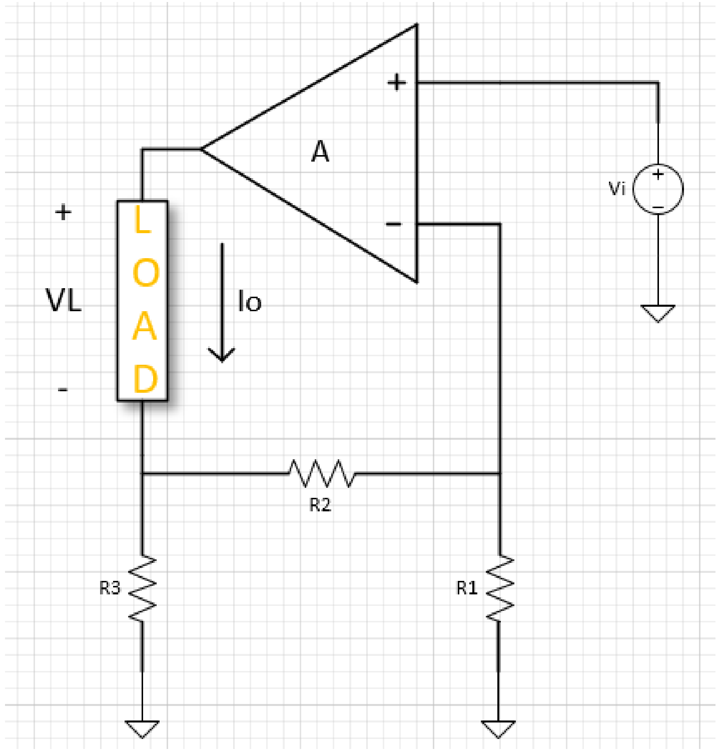

Figure 11

15. Assuming the op-amp of figure 12 has $r_d = \infty$, $A = 10^3\ V/V$ and r_0=0, and all resistance are identical.
    a) Find A_{ideal} and gain error GE.
    b) Find A_{min} for GE ≤ 0.1%. [Ans. a) A_{ideal} = -8 V/V, GE = 1.28%, b) A_{min} =13000 V/V]

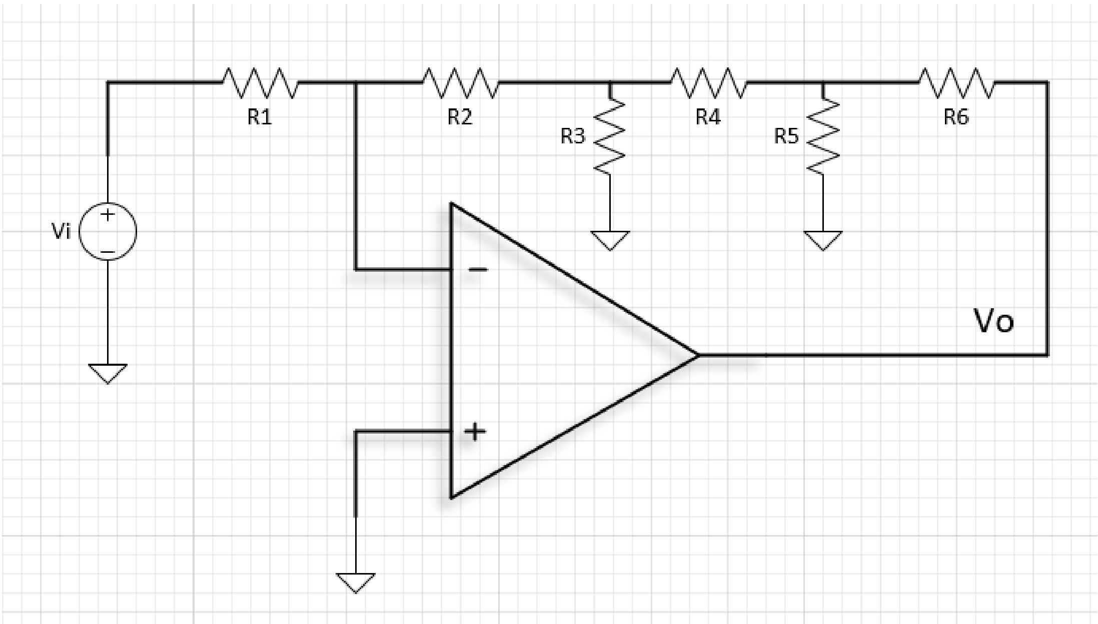

Figure 12

16. The circuit in figure 13 yields $I_0 = AV_I - (1/R_0)V_L$. Find the expression for A and R_0, as well as the condition among its resistances that yields R_0=∞.

[Ans. $A = \frac{(R_1+R_2)R_4}{R_1R_5(R_3+R_4)}$,$R_0 = \frac{R_5R_1(R_3+R_4)}{R_1R_4-R_2R_3}$, $R_0 \rightarrow \infty$ for $R_1R_4 = R_2R_3$]

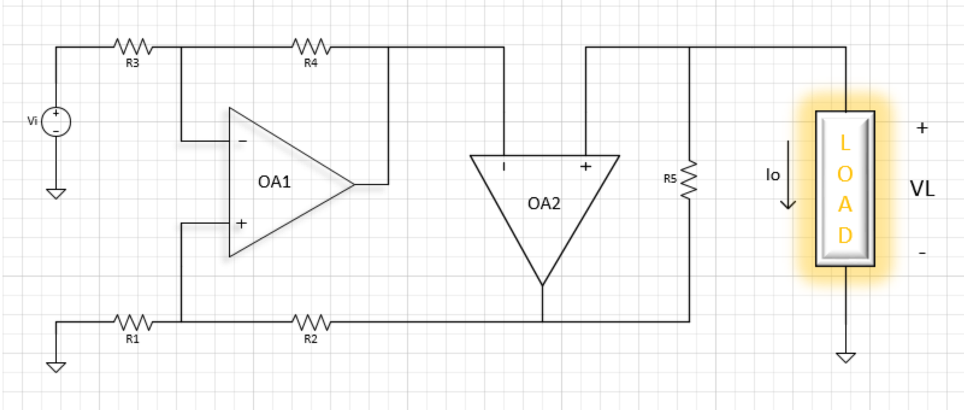

Figure 13

17. Show that the linearized bridge circuit of figure 14 yields $V_0 = R_2V_{REF}\,\delta/R_1$.

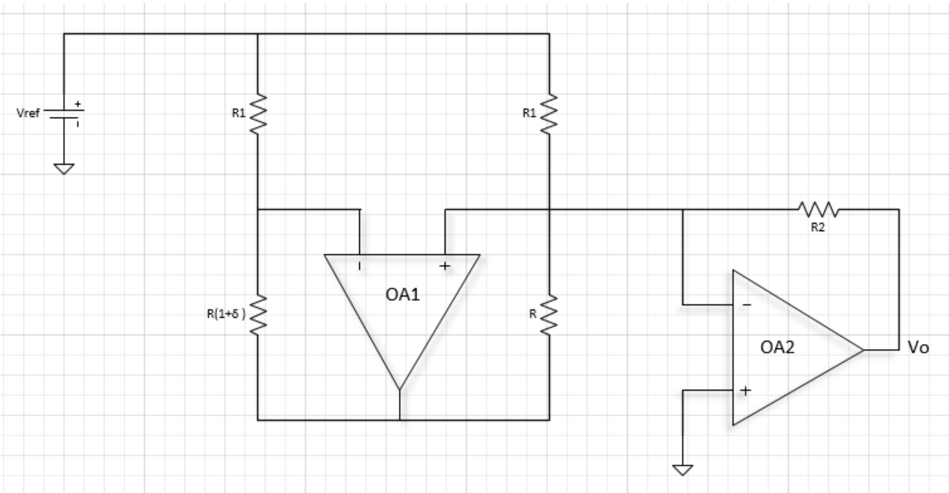

Figure 14

- **<u>Phase-lead/Phase-lag circuit:</u>**

18. Determine the phase angle and the time delay for the circuit shown in the figure 15 for a frequency of 2 kHz. Given: R_1= 20 kΩ, R= 39 kΩ, R_f= R_1 and C= 1nF.

[Ans. ϕ = 52.2^o, τ_d = 72.5 μs]

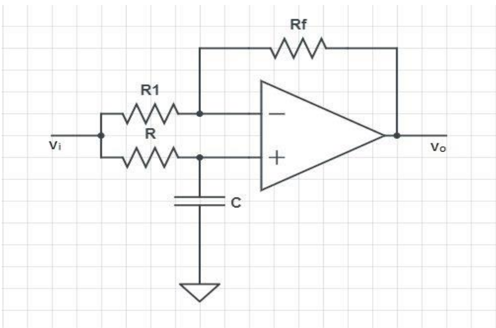

Figure 15

- **Slew rate limitations:**

19. An op-amp used as an inverting amplifier with a gain of 50. The voltage gain vs. frequency curve has a flat gain up to 20 kHz and SR=0.5 V/ µS. What maximum peak-to-peak input signal can be applied without distorting the output? [Ans. 3.98 V]

20. A square wave of peak-to-peak amplitude of 500 mV has to be amplified to a peak-to-peak amplitude of 3 V with a rise time of 4 µS or less. Is an op-amp with slew rate of 0.5 V/µS sufficient? [Ans. SR = 0.6 $V/\mu s$]

21. a) An op-amp has a slew rate of 2 V/µS. What is the maximum frequency of an output sinusoid of peak value 5 V at which distortion sets in due to slew rate limitation?
    b) If a sinusoid of 10 V peak is specified, what is the full power bandwidth?
    [Ans. a) 63.7 kΩ. b) 31.85 kΩ]

22. An op-amp has slew rate of 2 V/µS. Find the rise time for an output voltage of 10 V amplitude resulting from a rectangular pulse input if the op-amp is slew rate limited. [Ans. 4 µs]