EE60032: Analog Signal Processing

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Course Information

- **Course page:**

  http://www.facweb.iitkgp.ac.in/~ashismaity/Analog_Signal_Processing_Autumn_2020.html

- **References:**

1. Linear Integrated Circuits by D. Roy Choudhury and Shail B. Jain, New Age International Publisher
2. Analog Integrated Circuit Design, (2nd Edition) by Tony Chan Carusone, David Johns, Kenneth Martin, Wiley
3. Design with Operational Amplifiers and Analog Integrated Circuits by Sergio Franco (Fourth Edition), McGraw Hill Education
4. Analog Filter Design by Rolf Schaumann, Haiqiao Xiao, Mac Van Valkenburg, (Second Indian Edition), Oxford University Press
5. Fundamental of Microelectronics by Bezad Razavi, Wiley
6. Microelectronic Circuits by Sedra and Smith, (Fifth Edition), Oxford Indian Edition
7. CMOS Analog Circuit Design by Allen and Holberg, Oxford Indian Edition
8. Design of Analog CMOS Integrated Circuits by Bezad Razavi, Tata McGraw-Hill

- **Register yourself in Moodle.**

Tentative Systematic Evaluation Criteria

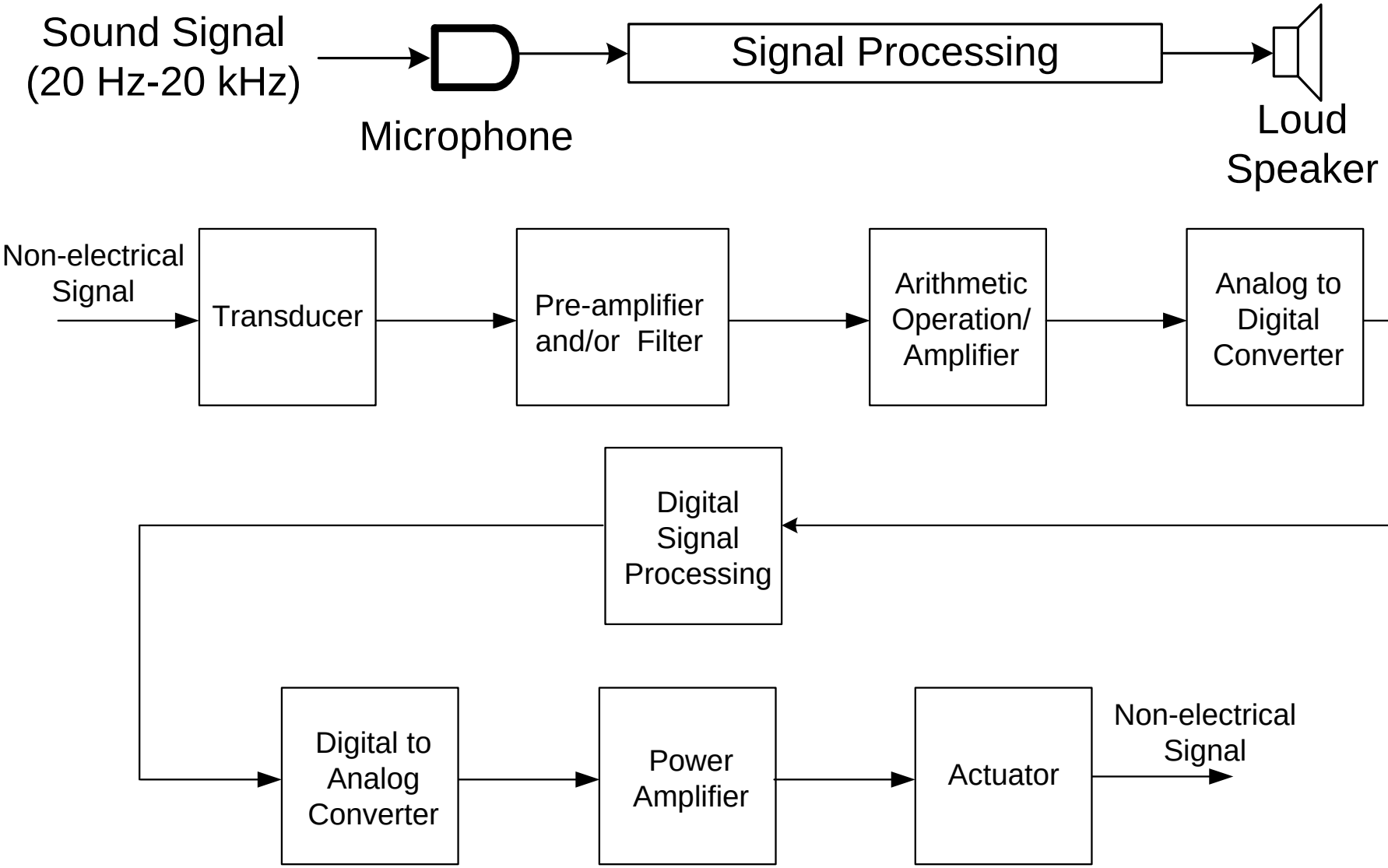
1. **Try yourself: 30%**
   - ✓ Meet the strict deadlines: Every Saturday by 11:59 PM.
   - ✓ Those who have internet connectivity issue, plan to submit early.
2. **Class Tests on Each Module: 40%**
   - ✓ After completion of each module, one class test will be conducted.
3. **Class Test on Whole Syllabus: 30%**
   - ✓ At the end, one class test on whole syllabus will be conducted.

This is a tentative plan. Based on pandemic situation, it may change.

Course Introduction

1. Course Objective:
   - ✓ Provides a system level (not IC level) perspective of Analog Signal Processing
   - ✓ Study different blocks involved in signal processing except DSP.
   - ✓ After this course, the students will be able to design the whole chain in system level except the processing in digital domain. Such processing are taught in DSP class.
2. Course Name: Analog Signal Processing
3. What is signal?
4. Why analog signal?
5. Why do we need processing?

Example of simple system and its basic building blocks



Brief contents of the course

- Module-1: Signal processing using operational amplifier
- Module-2: Analog and switched capacitor filters
- Module-3: Data converters
- Module-4: Oscillator and Phase locked loop
- Module-5: Noise

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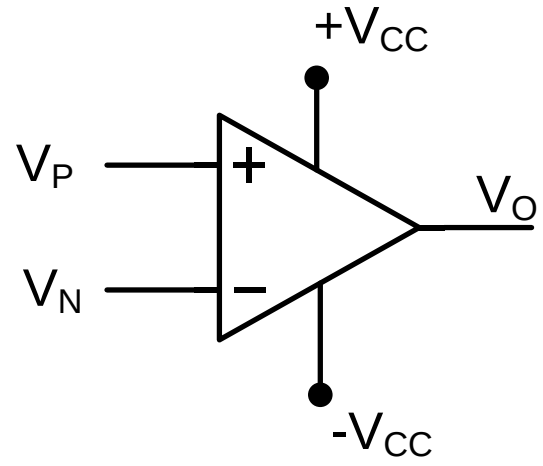
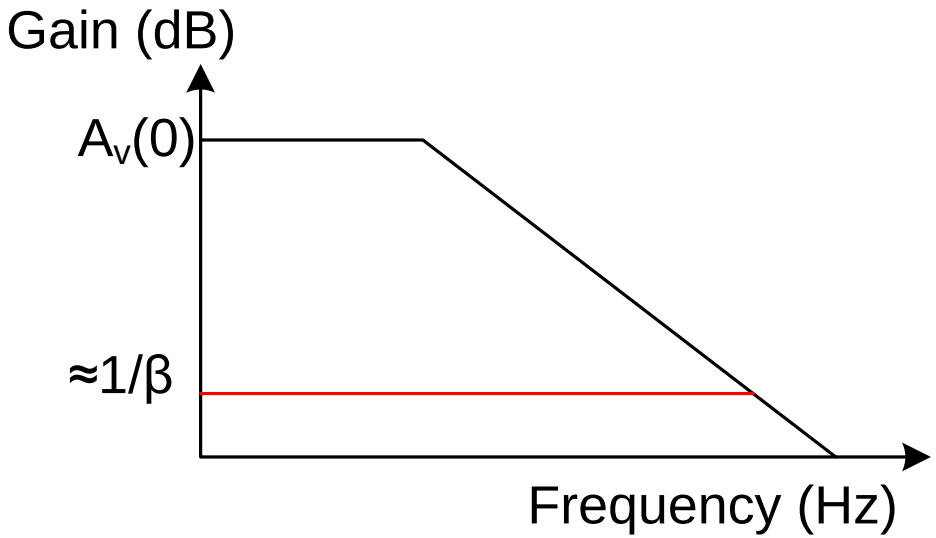
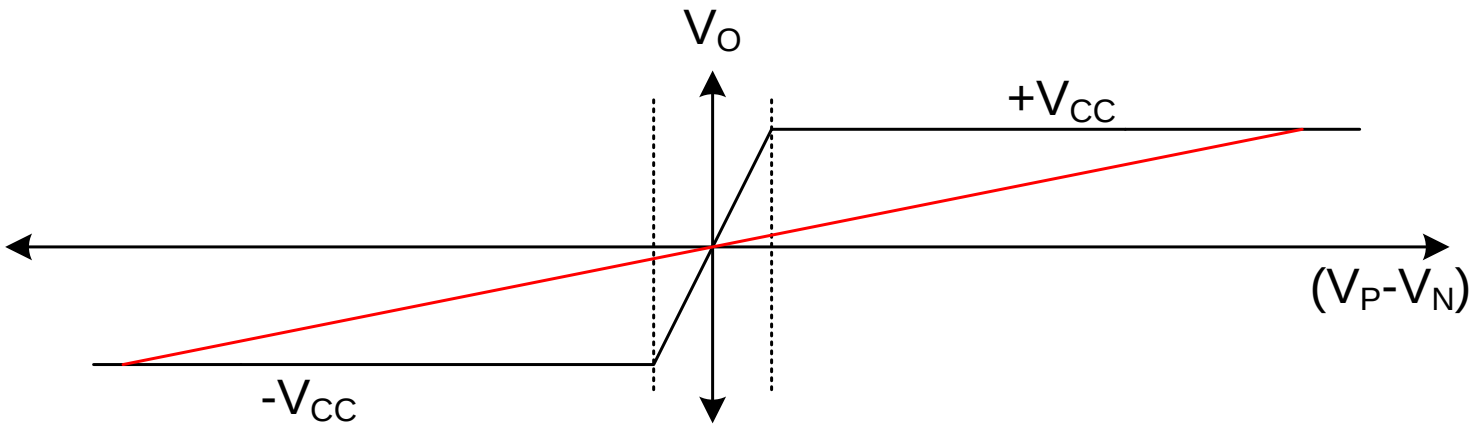
Module-1: Signal processing using operational amplifier

Operational amplifier

- The symbols of a comparator and an op-amp are the same
- Is there any fundamental difference in operation?
  - Op-amp operates in closed loop whereas the comparator operates in open-loop configuration. Exception: Schmitt trigger
  - Their region of operations are different. Op-amp operates in small signal domain whereas the comparator in large signal.

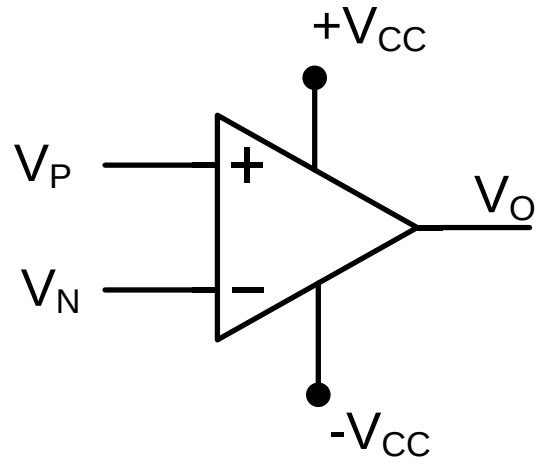






Operational amplifier

- **Properties of an ideal op-amp:**
  - Infinite dc (open-)loop gain, $A_v(0)=\infty$
  - Infinite loop bandwidth, $f_{BW}=\infty$
  - Infinite input impedance, $R_i=\infty$
  - Zero output impedance, $R_o=0$

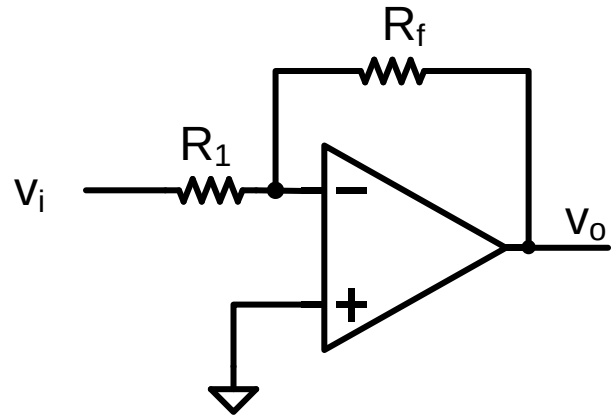


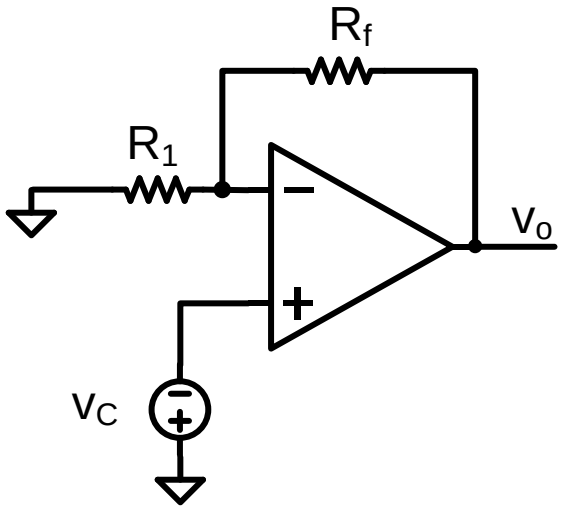
Ideal op-amp does not exist! Then, what is the significance?

- **Different non-idealities in op-amp:**
  - Input bias current, Input offset current, Input offset voltage: Mostly affect the DC performance
  - High dc (open-)loop gain, High loop bandwidth, High input impedance, Low output impedance: Mostly affect the AC performance

Non-idealities: Input bias current

- Assumption: Bias currents are equal, i.e., $I_B^{(+)}=I_B^{(-)}$
- How much output offset is getting created?
  - If $v_i=0$, $v_o=+I_B^{(-)}R_f$
  - Example: $R_f=1\ M\Omega$, $I_B^{(-)}=500\ nA$, $v_o=500\ mV$
- How to compensate the output offset due to input bias current?



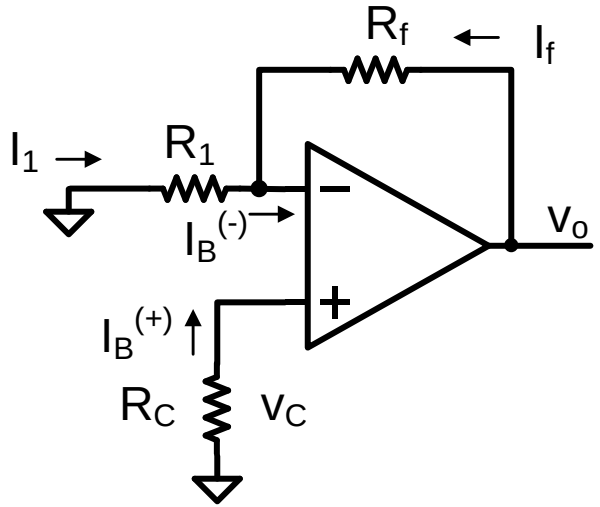


Conceptual development

Try yourself!

$R_C=R_1||R_F$

Hint: R_1 will carry current

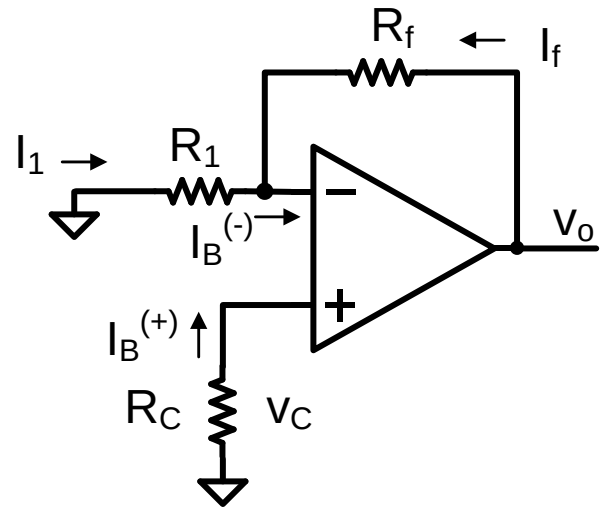


Practical implementation

Non-idealities: Input offset current

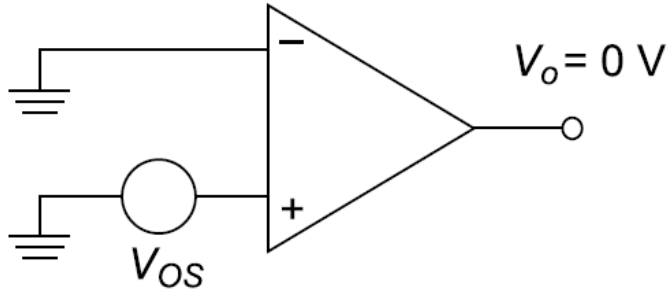
- Assumption: Bias currents are equal, i.e., $I_B^{(+)} \neq I_B^{(-)}$ and $|I_{OS}| = I_B^{(+)} - I_B^{(-)}$
- How much output offset is getting created?
  - $v_C = I_B^{(+)} R_C$,
  - $I_1 = v_C / R_1 = I_B^{(+)} R_C / R_1$
  - $I_1 + I_f = I_B^{(-)}$
  - Try yourself!

    $v_O = R_f I_{OS}$



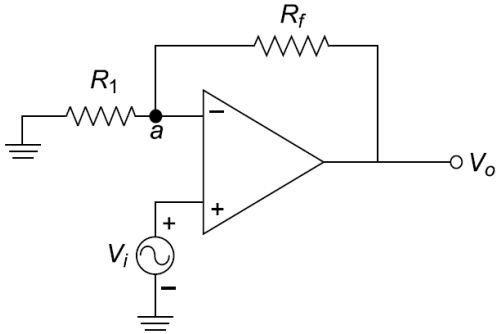
Non-idealities: Input offset voltage

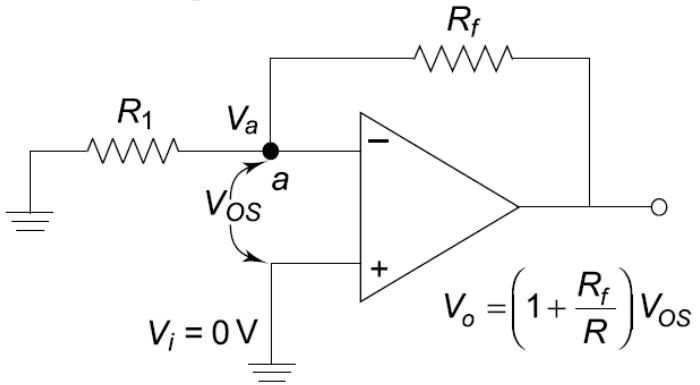
- **Input offset voltage can arise for different reasons:**
  - ✓ **Input pair mismatch**
  - ✓ **Output transistors mismatch**



Op-amp with input offset voltage with any polarity

- **How to quantify?**
  - ✓ **Differential input voltage between inverting and non-inverting terminal.**
  - ✓ **Voltage to be applied to make output zero.**
- **What is its implication at the output?**





Try yourself!

Calculate the output voltage due to input offset of an inverting amplifier

Non-inverting amplifier and calculation of output voltage due to input offset

Calculation of total output offset voltage

- **Total offset voltage due to input bias current, input offset current and input offset voltage**
  - **If compensating resistance Rc is not used:**

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_B$$

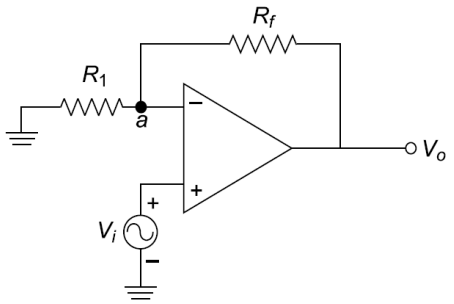
    - ✓ Assumption: input offset current I_{OS} < input bias current I_B
    - ✓ Depending on the polarity of V_{OS}, the associated term could be positive or negative
  - **If compensating resistance is used:**

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_{OS}$$

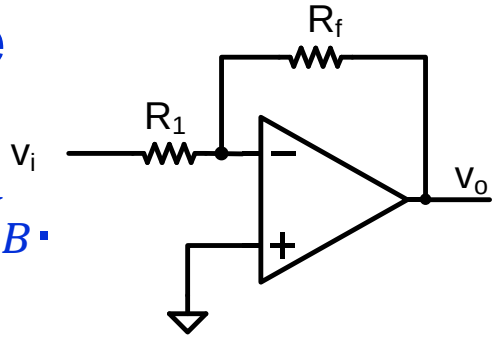
    - ✓ As $I_{OS} < I_B$, the use of R_C reduces the offset voltage.

Try Yourself: Tutorial Problems

1. For the non-inverting amplifier as shown in the figure, R_1 = 1 KΩ, R_f = 10 KΩ.
   a) Calculate the maximum output offset voltage due to V_{ios} and I_B. Assume the op-amp has V_{ios} = 10 mV, I_B = 300 nA and I_{os} = 50 nA.
   b) Calculate the value of R_{comp} needed to reduce the effect of I_B.
   c) Calculate the maximum output offset voltage if R_{comp} as calculated in (b) is connected in the circuit.

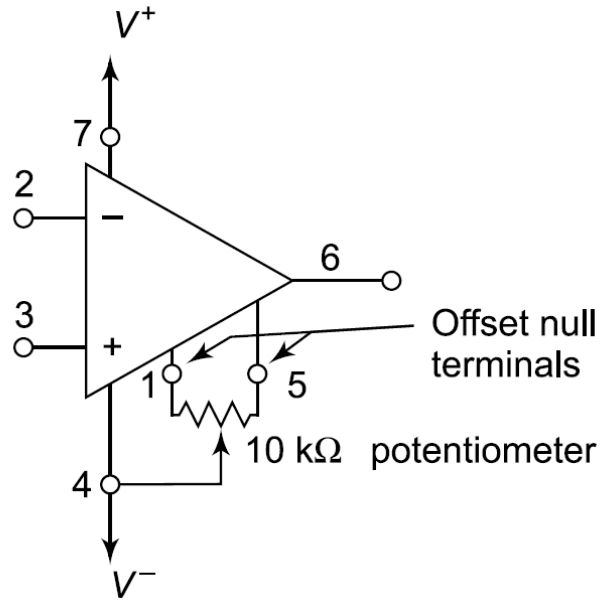


2. In an inverting amplifier R_1 = 100 KΩ, R_f = 10 MΩ and V_{ios} = 6 mV and I_B = 500 nA.
   a) Calculate maximum output offset voltage caused by input offset voltage V_{ios}.
   b) Calculate maximum output offset voltage caused by input bias current I_B.



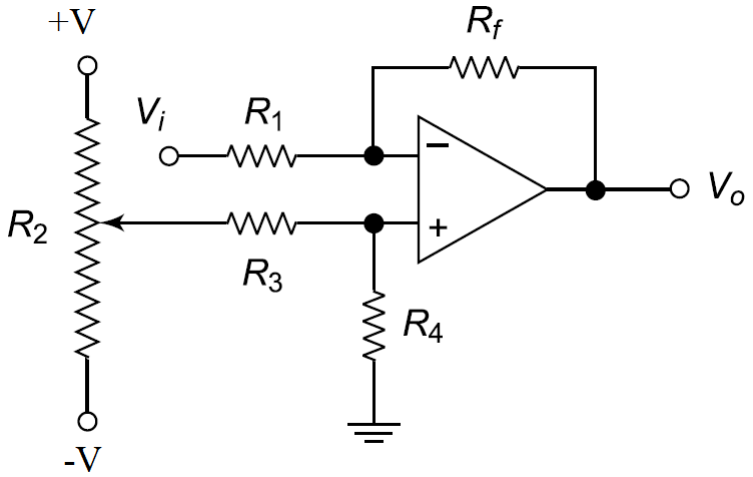
Offset Voltage Compensation

- **When offset compensation pin is available:**



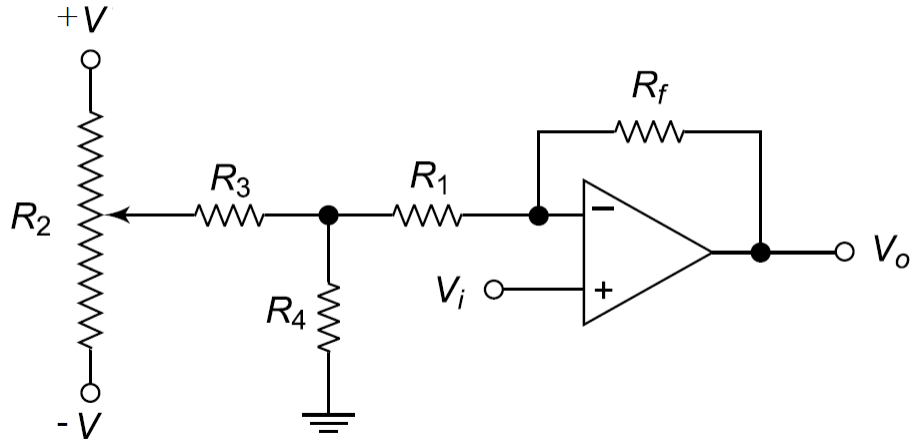
Offset compensation network in 741 op-amp

- **When no offset null pins are available:**



External offset compensation network in an inverting amplifier

$$V_{OS} = \pm V\left(\frac{R_4}{R_3 + R_4}\right)$$



External offset compensation network in a non-inverting amplifier

$$V_{OS} = \pm V\left(\frac{R_4}{R_4 + R_3}\right)$$

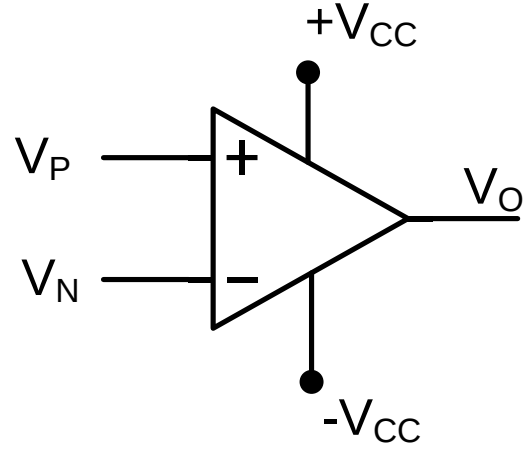
- ✓ $R_4 \ll R_3$
- ✓ **Example: R_4=100 Ω, R_3=100 kΩ, V=15 V, then -15 mV ≤V_{OS} ≤ +15 mV**

Thermal Drift

1. I_B, I_{OS}, V_{OS} are not constant for a given op-amp. Rather, they can vary:
   a) Over temperature
   b) Over supply voltage
   c) Over time
2. Temperature causes most serious issues.
3. Thermal drift is defined as the average rate of change of a particular quantity per unit change in temperature. For examples: $\Delta I_B/\Delta T$ (pA/^{O}C), $\Delta I_{OS}/\Delta T$ (pA/^{O}C), $\Delta V_{OS}/\Delta T$ (μV/^{O}C),
4. It is not a constant value and usually non-uniform/non-linear over temperature range.
5. So, a circuit nulled at 25^{O}C, may not remained nulled at other temperature.
6. Datasheet usually specify the average or maximum thermal drift.

Power Supply Rejection Ratio (PSRR)

1. Op-amp output is sensitive to the power supply voltage.
2. Power Supply Rejection Ratio (PSRR)=Change in Supply voltage/Change in output voltage.
3. PSR=$20\log_{10}$(PSRR)
4. Datasheet gives DC PSR as well as AC PSR performance.



Try Yourself: Consider an op-amp with PSR of 90 dB. When the op-amp is operated with a power supply gets a voltage step of 0.5 V, find out the change at the output of the op-amp.

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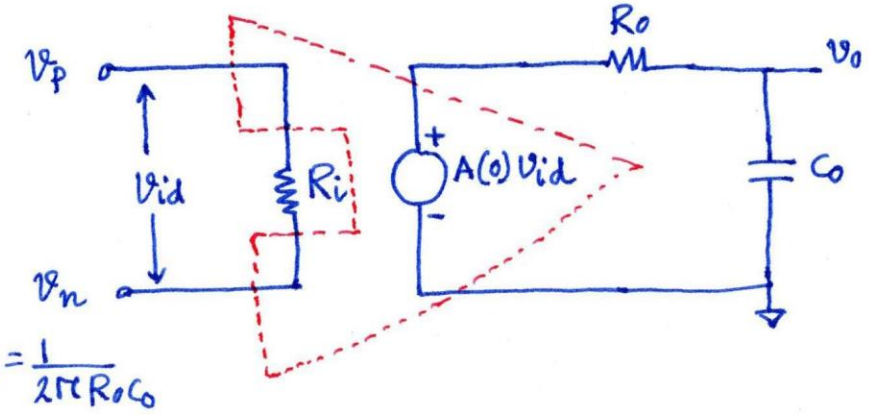
AC Performance of the op-amp

$$v_o = \left(\frac{\frac{1}{j\omega C_o}}{R_o + \frac{1}{j\omega C_o}} \right) A(0)\, v_{id}$$

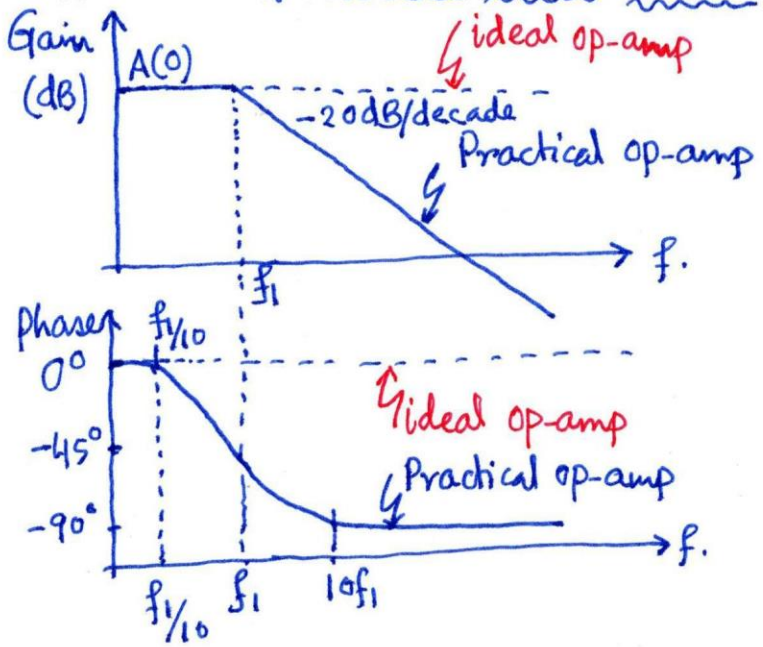
Open loop gain $A(s) = \frac{v_o}{v_{id}} = \left(\frac{1/j\omega C_o}{R_o + \frac{1}{j\omega C_o}} \right) A(0)$

$$= \frac{A(0)}{1 + j\omega R_o C_o} = \frac{A(0)}{(1 + j\, f/f_1)} \quad \text{where } f_1 = \frac{1}{2\pi R_o C_o}$$

$$|A(s)| = \frac{A(0)}{\sqrt{1 + (f/f_1)^2}} \quad \text{and} \quad \angle A(s) = -\tan^{-1}(f/f_1)$$

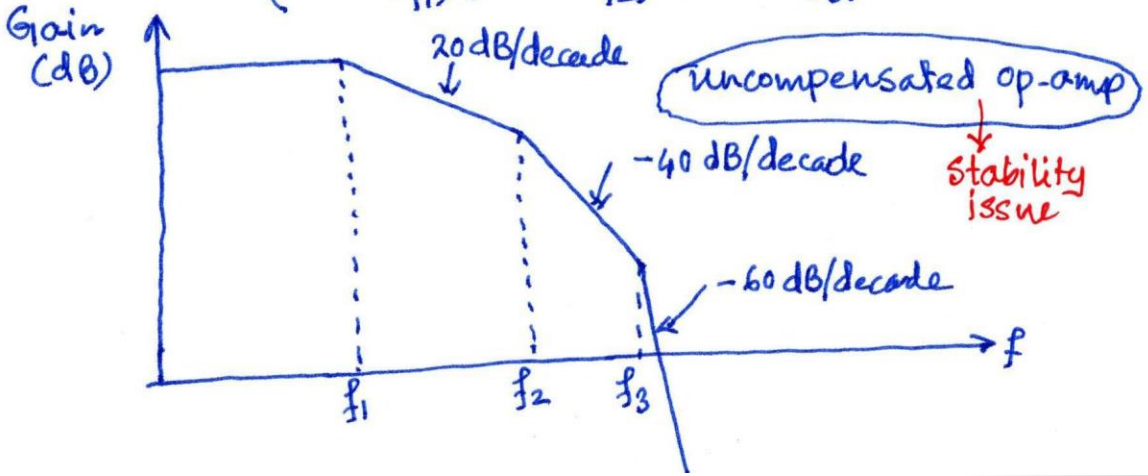


● How the gain and phase plots changed ?



● Practical op-amp has multiple number of stages and each stage contributes one pole.

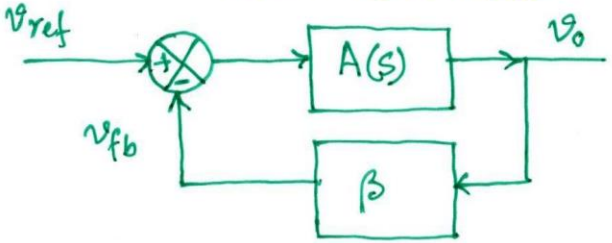
$$A(s) = \frac{A(0)}{(1 + j\, f/f_1)(1 + j\, f/f_2)(1 + j\, f/f_3)} \qquad f_1 < f_2 < f_3$$



Stability of an op-amp

* As op-amp will be connected in feedback configuration, we have to ensure stability of loop.

Basic feedback theory :-



Phase margin = $180° - \angle \beta A(s)$

$$A_{CL}(s) = \frac{A(s)}{1 + \beta A(s)}$$

If the characteristic equation $1 + \beta A(s) = 0$, then it is not stable.

Here, loop gain = $\beta A(s)$ → (Open-) loop gain

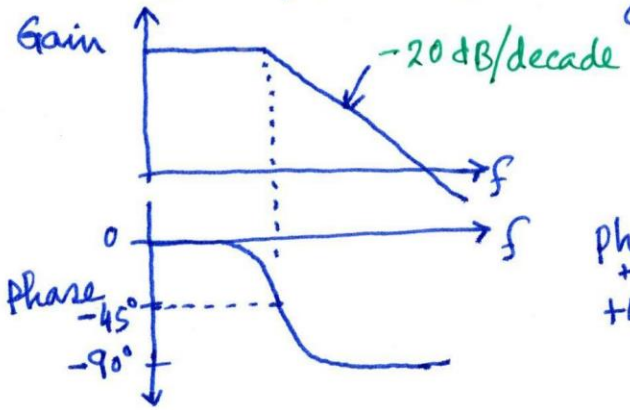
If $\beta A(s) = -1$, then it becomes positive feedback.

$|\beta A(s)| = 1$ and $\angle -\beta A(s) = 0$ (or multiple of 2π)

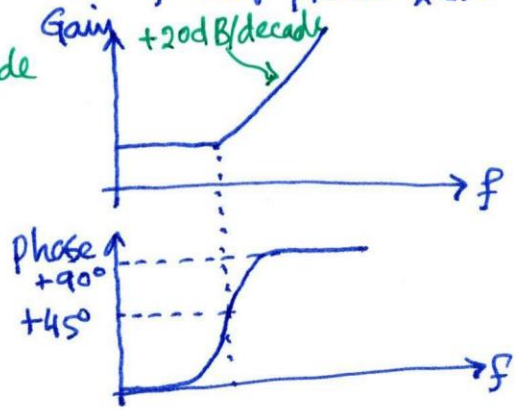
$\angle \beta A(s) = \pi$ (or multiple of π)

AC response of a pole and zero :-

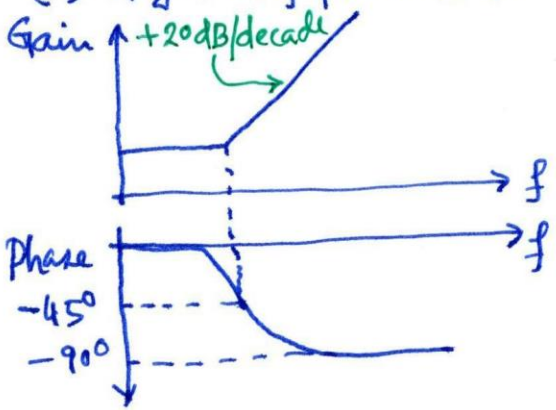
i) Left half plane pole



ii) Left half plane zero



(iii) Right half plane zero



Observations :-

a) Gain plot of a pole and zero differs

b) RHP zero has same phase char. as LHP pole

c) LHP pole can be cancelled by LHP zero.

If we have multiple low frequency poles, phase margin will be negative. Hence, system will be unstable.

Frequency Compensation

- Two types of compensation techniques: (i) External compensation → Dominant pole compensation
  (ii) Internal compensation → Pole-zero compensation

- External compensation :-

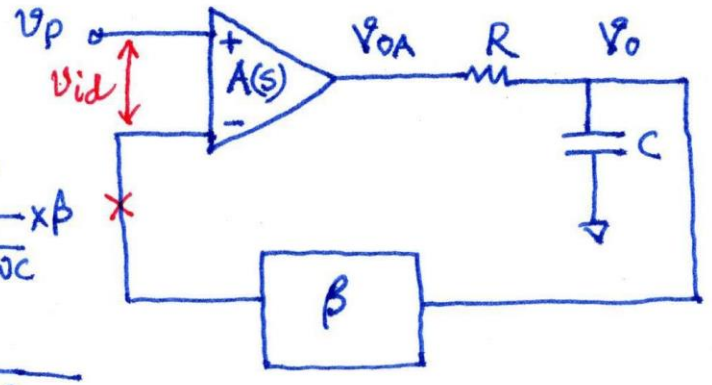
(i) Dominant pole compensation :-

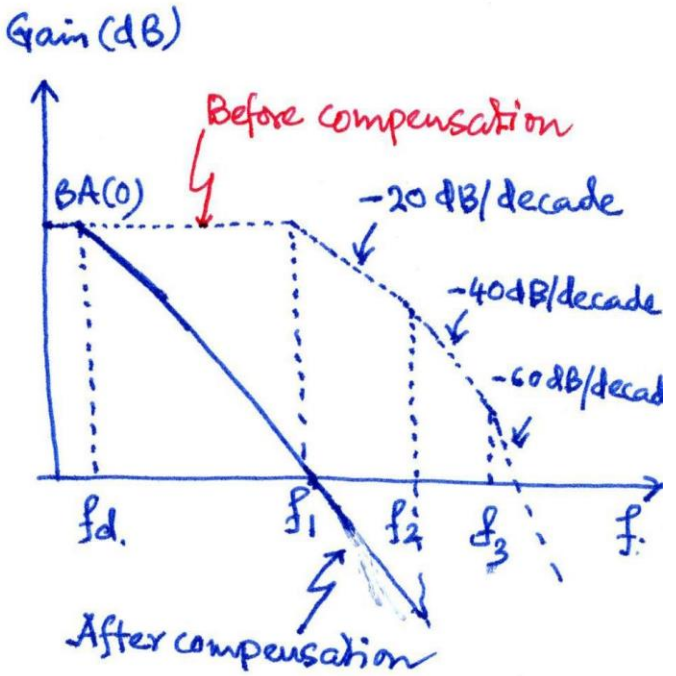
$$\text{Loop gain} = \frac{v_{oA}}{v_{id}} \times \frac{v_o}{v_{oA}} \times \beta$$

$$= \frac{A(0)}{(1+j f/f_1)(1+j f/f_2)(1+j f/f_3)} \times \frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}} \times \beta$$

$$= \frac{BA(0)}{(1+j f/f_d)(1+j f/f_1)(1+j f/f_2)(1+j f/f_3)}$$

where $f_d = \frac{1}{2\pi RC}$ and $f_d < f_1 < f_2 < f_3$





Disadvantage : BW is reduced drastically.

Advantage : Noise immunity increases.

Design tips :-

If $f_1 = f_{UGF}$, then Phase margin = 45°

If $f_1 = 2.2\, f_{UGF}$, then phase margin = 60°

If $f_1 \geq 10\, f_{UGF}$, then phase margin = 90°

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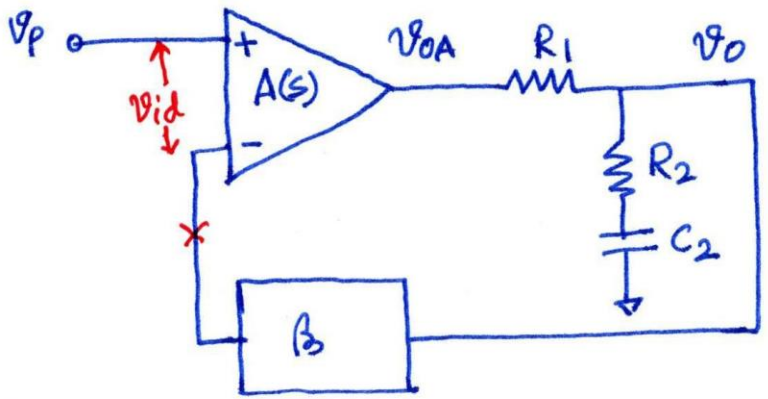
(ii) Pole-zero compensation (also known as Lag compensation) :-



$$\frac{v_o}{v_{oA}}(s) = \frac{R_2 + 1/sC_2}{R_1 + R_2 + \frac{1}{sC_2}} = \frac{1 + sR_2C_2}{1 + sC_2(R_1+R_2)} = \frac{\left(1 + j\, f/f_z\right)}{\left(1 + j\, f/f_x\right)}$$

where, $f_z = \frac{1}{2\pi R_2 C_2}$ and $f_x = \frac{1}{2\pi (R_1+R_2) C_2}$

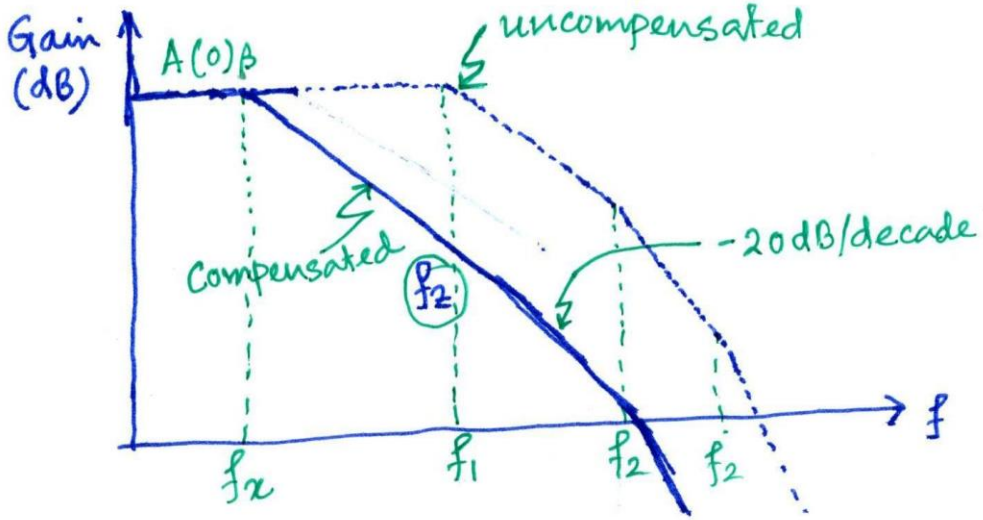
$f_x < f_z \Rightarrow$ pole appears before zero.

$$\text{Loop gain} = \frac{v_o}{v_{oA}} \times \frac{v_{oA}}{v_{id}} \times B = \frac{A(0)B\left(1 + f/f_z\right)}{\left(1 + j\, f/f_1\right)\left(1 + j\, f/f_2\right)\left(1 + j\, f/f_3\right)\left(1 + j\, f/f_x\right)}$$

Design strategy :-

1) $f_x < f_1 < f_2 < f_3$

2) f_1 will be cancelled by f_2 → pole-zero cancellation.



Advantage :-

Achieved UGF is high compared to dominant pole compensation.

Disadvantage :

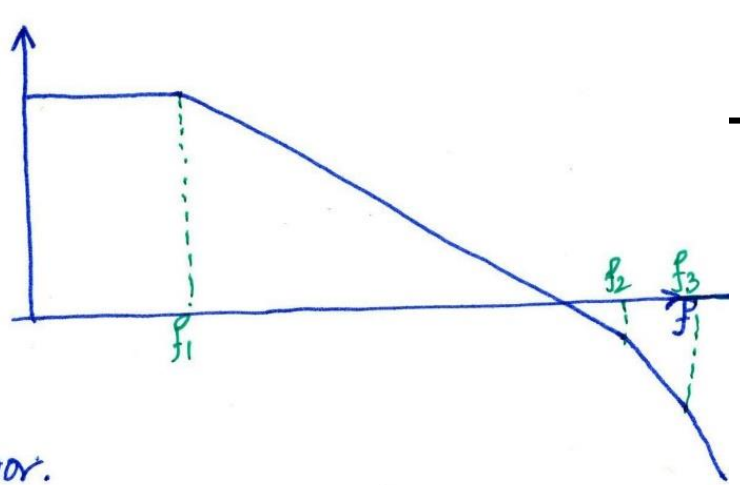
Perfect pole-zero cancellation is not possible due to component variation.

2) Internal Compensation :-

For low speed application, it is used.

While designing the op-amp ckt, it is over-compensated.

$$\text{Loop gain} = \frac{BA(0)}{(1+j\,f/f_1)(1+j\,f/f_2)(1+j\,f/f_3)}.$$



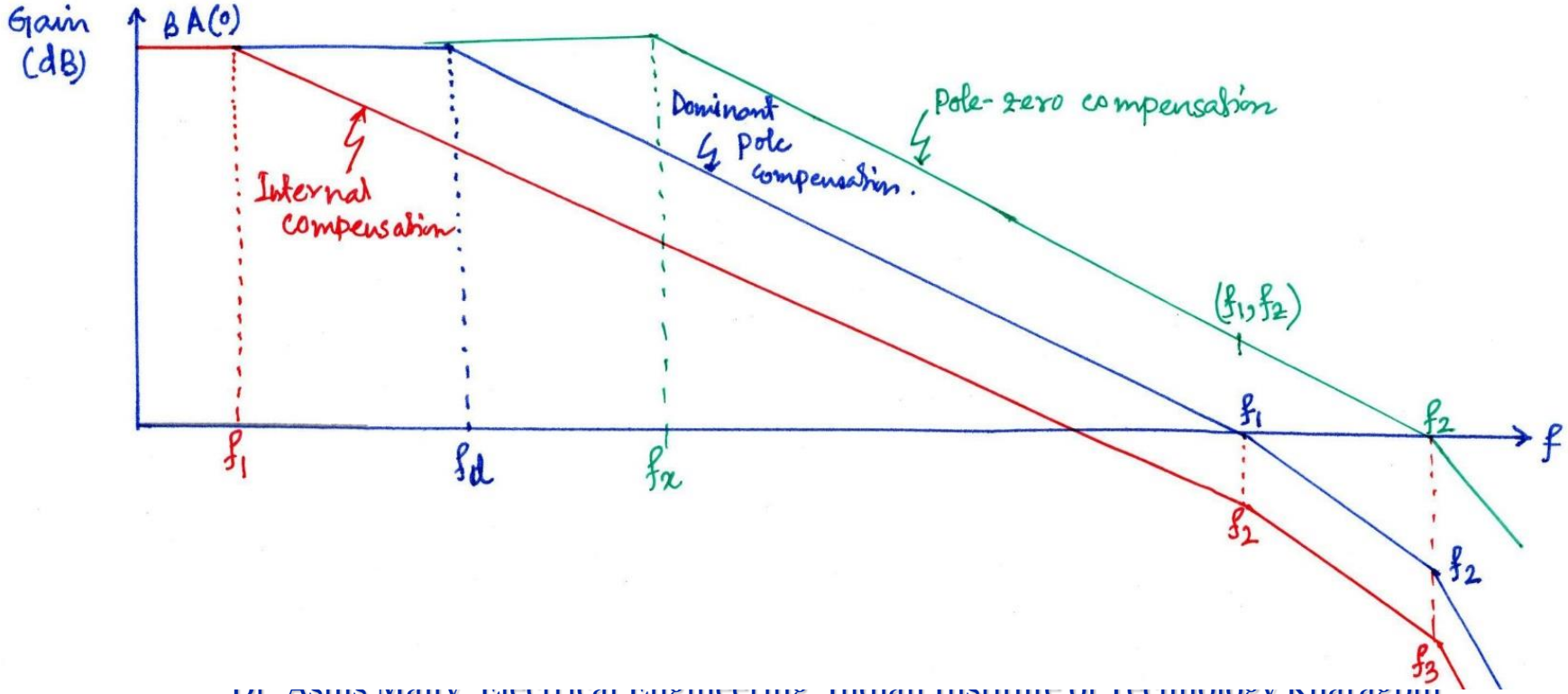
Advantage :-

No extra compensation ckt is required externally.

Disadvantage :

Very limited bandwidth, speed of operation is poor.

● Comparison between different compensation scheme :-

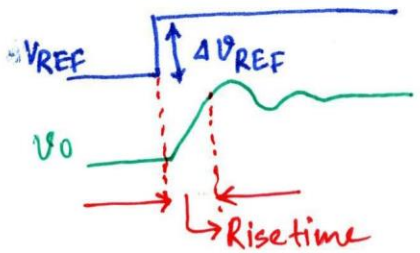


Few observations :-

1) If op-amp is uncompensated, external compensation needs to be used first.
2) Once compensated, it gets approximated to either single pole or two pole systems.
3) For 45° phase margin, second pole is placed at unity gain frequency f_{UGF} } Two pole system
   For 60° phase margin, second pole is placed at 2.2 times of f_{UGF}
   For 90° phase margin, second pole is placed at >10 times of f_{UGF} → approximated as single pole system

How $f_{3dB,CL}$ affects transient response :-

$f_{3dB,CL}$ is a small signal parameter and it influence only the small signal response.



when small signal step ΔV_{REF} is applied, V_o will also change.

Rise time is time taken from 10% to 90% of final value.

$$f_{3dB,CL} \approx \frac{0.35}{\text{Rise time}}$$

Importance of gain-bandwidth product :- (in a compensated op-amp)

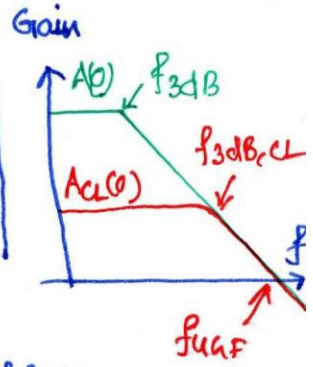
Open loop bandwidth = f_{3dB} (or first pole)

Open loop gain = $A(0)$

Closed loop bandwidth = $f_{3dB,CL}$

Closed loop gain = $A_{CL}(0)$

$$f_{3dB} \times A(0) = f_{3dB,CL} \times A_{CL}(0) = f_{UGF}$$



Try yourself :-

1) An op-amp has a small signal rise time of 0.7 μs. Determine $f_{3dB,CL}$.
2) 741 op-amp has $f_{3dB} = 5$ Hz, $A(0) = 200,000$. If a closed loop amplifier is developed using 741 op-amp having $A_{CL}(0) = 10$, find out $f_{3dB,CL}$.

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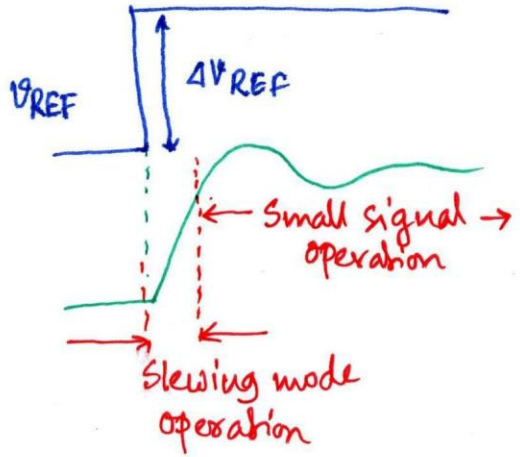
Slew rate limitation

Slew rate is a large signal phenomena.



What is slew rate of an op-amp :-

Max. rate of change of the output voltage.

Lets assume, output capacitor C_o.

$Q = CV$.

$i_g dt = C_o dv_o$

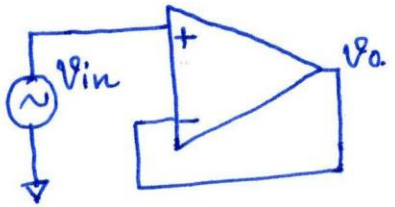
$$\boxed{\frac{dv_o}{dt} = \frac{i_g}{C_o}}$$

Example :-

If max charging/discharging current is $15\mu A$, $C_o = 20\,pF$

$SR = \frac{15\mu}{30p} = 0.5\,V/\mu s.$

How slew rate affects in signal processing :-



Input signal V_{in} may have slew rate (or maximum slew rate)

$v_{in} = V_m \sin\omega t$ → For sinusoidal input

$v_o = v_m \sin\omega t$ → because of unity gain configuration

$\frac{dv_o}{dt} = V_m \omega \cos\omega t$. → Desired output slew rate

Max. rate of change of the O/p occurs when $\cos\omega t = 1$.

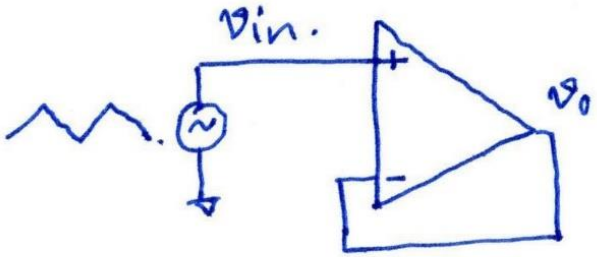
Max slew rate $SR_{max} = \left.\frac{dv_o}{dt}\right|_{max} = V_m\omega. = 2\pi f V_m$ V/S.

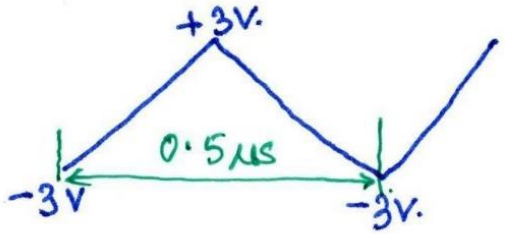
* Op-amp slew rate SHOULD be higher than max. slew rate at the O/p as desired by I/p signal without creating no distortion.
* If $f\uparrow$, SR of the op-amp needs to be increased. → $f_{max} = \frac{SR}{2\pi V_m}$.
  If $V_m\uparrow$, SR of the op-amp needs to be increased.

Slew rate requirement also changes based on input signal.

Example :-

1) The output of a voltage follower is a triangular waveform, having 6 V peak-to-peak of 2 MHz. What would be the required slew rate of the op-amp to get an undistorted output?





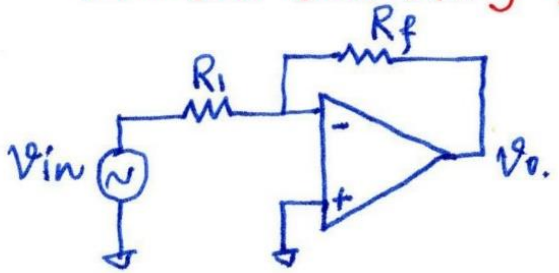
$$\text{Output signal slew rate} = \frac{dV_o}{dt}$$

$$= \frac{6\text{ V}}{\frac{0.5\,\mu}{2}} = \frac{12\text{ V}}{0.5\,\mu}$$

$$= 24\text{ V/}\mu\text{s}$$

So, the desired slew rate of the op-amp $\geq$ 24 V/μs

2) An inverting op-amp has a gain of −50. The gain curve has a flat gain upto 20 kHz. and slew rate SR = 0.5 V/μs. What maximum peak-to-peak input signal can be applied without distorting the output? Consider a sinusoidal input signal.



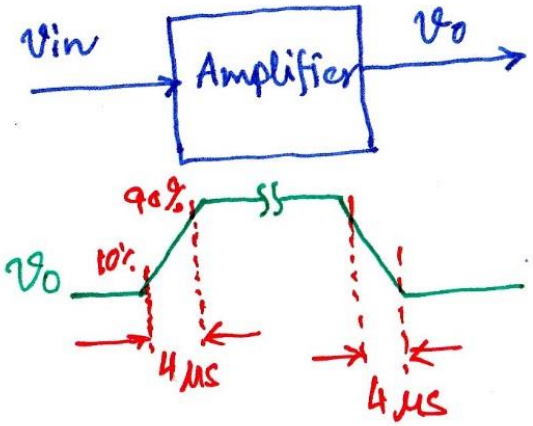
For sinusoidal o/p, $V_m = \frac{SR}{2\pi f_{max}} = \frac{0.5\text{ V}/\mu\text{s}}{2\pi \cdot 20\text{ kHz}} = 3.98\text{ V}$ peak.

peak-to-peak o/p voltage = $2 \times 3.98\text{ V} = 7.96\text{ V}$.

peak-to-peak i/p voltage = $\frac{7.96}{50} = 159\text{ mV}$.

Example :-

3) A square wave of peak-to-peak amplitude of 500 mV has to be amplified to a peak-to-peak amplitude of 3V with a rise time of 4 μs or less. Is an op-amp with a slew rate of 0.5V/μs sufficient?



Required slew rate of o/p signal = $\frac{dv_o}{dt}$.

Rise time ⟶ time taken to rise from 10% to 90% of the final value

10% of v_o = 0.3V.

90% of v_o = 2.7V.

$dv_o = 2.7 - 0.3 = 2.4V$. and $dt = 4\mu s$.

$\frac{dv_o}{dt} = \frac{2.4\ V}{4\ \mu} = 0.6\ V/\mu s.$ < op-amp slew rate (0.5V/μs)

The slew rate of the op-amp is not sufficient.

Try yourself :

An op-amp has slew rate of 2V/μs. Find the rise time for an output voltage of 10V amplitude resulting from a rectangular pulse input considering the op-amp is slew rate limited.

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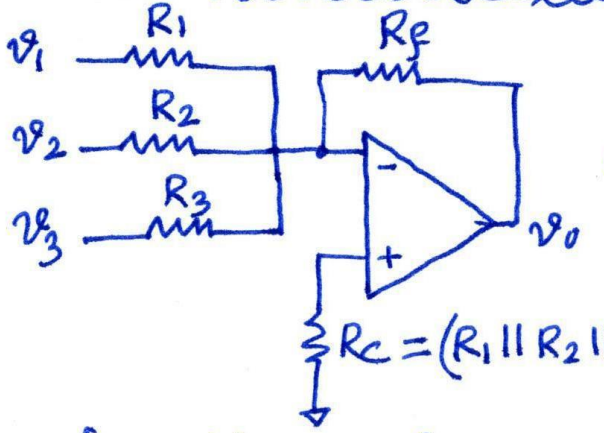
Applications of Op-amp in signal processing

(*) Summing amplifier/Adder :-



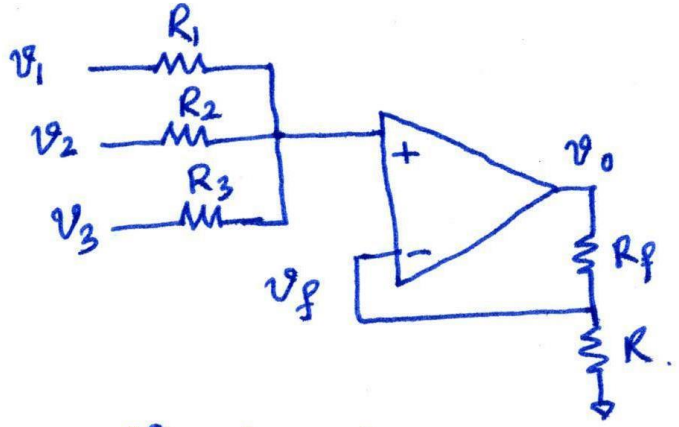
Inverting configuration

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} + \frac{v_0}{R_f} = 0$$

or, $$v_0 = -\left[\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f v_3}{R_3}\right]$$

If $R_1 = R_2 = R_3 = R_f$

$$\boxed{v_0 = -[v_1 + v_2 + v_3]}$$



Non-inverting configuration

$$\frac{v_1 - v_f}{R_1} + \frac{v_2 - v_f}{R_2} + \frac{v_3 - v_f}{R_3} = 0.$$

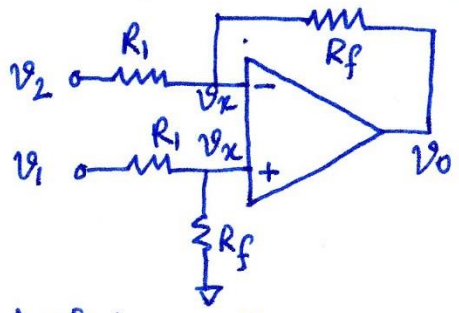
or, $$v_0 = \left(1 + \frac{R_f}{R}\right) \frac{v_1/R_1 + \frac{v_2}{R_2} + \frac{v_3}{R_3}}{1/R_1 + \frac{1}{R_2} + 1/R_3}$$

If $R_1 = R_2 = R_3$ & $\frac{R_f}{2} = R$.

$$\boxed{v_0 = v_1 + v_2 + v_3}$$

⊛ Subtractor / Difference Amplifier :-

✓ Very useful in differential signaling. If v_1 and v_2 are input signals, $v_{DM} = (v_1 - v_2)$, $v_{CM} = \frac{v_1 + v_2}{2}$



If $v_1 = 0$, $\frac{v_{o2}}{v_2} = -\frac{R_f}{R_1}$

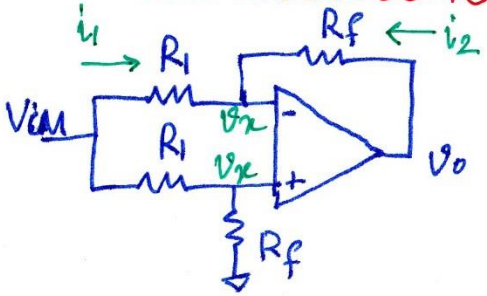
If, $v_2 = 0$, $\frac{v_x}{R_1} + \frac{v_x - v_{o1}}{R_f} = 0$ where $v_x = \left(\frac{R_f}{R_1 + R_f}\right) v_1$

or, $\frac{v_{o1}}{v_1} = \frac{R_f}{R_1}$

Applying voltage superposition: $v_o = v_{o1} + v_{o2} = \frac{R_f}{R_1} v_1 - \frac{R_f}{R_1} v_2 = \frac{R_f}{R_1}(v_1 - v_2)$

If $R_1 = R_f$, $\boxed{v_o = (v_1 - v_2)}$ and $\boxed{\frac{v_o}{v_1 - v_2} = \frac{R_f}{R_1}}$ → Differential gain (Ad)

What is the common mode gain :-



$v_x = v_{CM} \frac{R_f}{R_1 + R_f}$

$i_1 = \frac{(v_{CM} - v_x)}{R_1} = \frac{1}{R_1}\left[v_{CM} - \frac{v_{CM} R_f}{R_1 + R_f}\right] = \frac{v_{CM}}{R_1 + R_f}$.

$i_2 = \left(\frac{v_o - v_x}{R_f}\right) = \frac{1}{R_f}\left[-\frac{R_f}{R_1 + R_f} v_{CM} + v_o\right]$

As, $i_1 = -i_2$

$\frac{v_{CM}}{R_1 + R_f} = -\frac{1}{R_f}\left[v_o - \frac{R_f}{R_1 + R_f} v_{CM}\right] \Rightarrow v_o = 0$, Common mode gain $= 0$, $A_{CM} = 0$, $CMRR = \frac{\text{Diff. gain}}{\text{Common Mode gain}} = \infty$

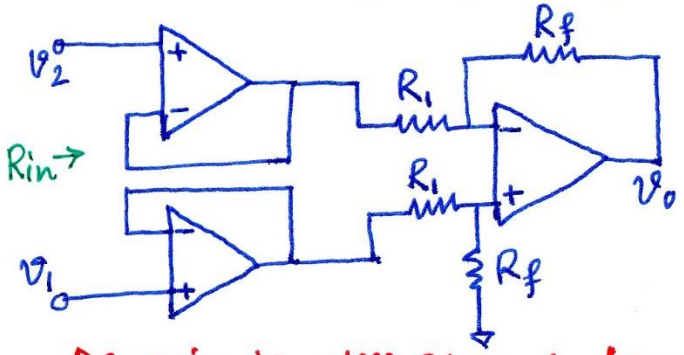
What is the input impedance of the circuit :-

$2R_1$

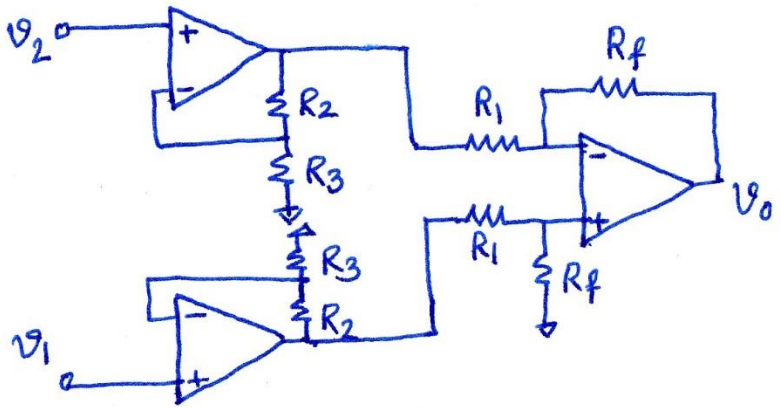
⊛ Limitation :- $A_d \uparrow$, $R_1 \downarrow$ → Unavoidable trade-offs.

Development of Instrumentation Amplifier

Step 1 : Improving input impedance. **Step 2 :-** Improving dc gain



DC gain is still limited $A_d = \frac{R_f}{R_1}$

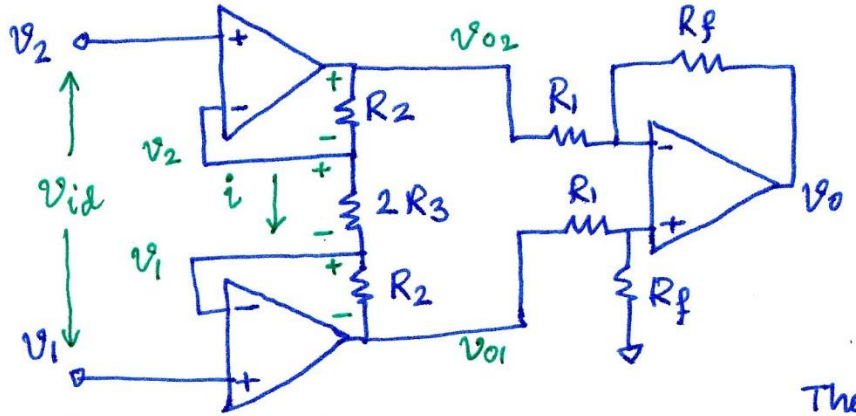


$$A_d = \left(1+\frac{R_2}{R_3}\right)\frac{R_f}{R_1}$$

First stage amplifies differential signal as well as common mode signal.

The output common mode of the first stage may be high or saturate.

Step 3 (Final modification) :- Eleminating common mode gain



$$v_1 = v_{ac1} + V_{CM}$$

$$v_2 = v_{ac2} + V_{CM}$$

$$v_{id} = (v_1 - v_2) = v_{ac1} - v_{ac2}$$

$$v_{id} = v_1 - v_2$$

$$i = \frac{v_2 - v_1}{2R_3} = -\frac{v_{id}}{2R_3}$$ [✓ independent of V_{CM} — common mode is suppressed]

$$v_{o2} = v_{o1} + i(R_2 + 2R_3 + R_2) = v_{o1} + i\,2(R_2+R_3)$$

$$= v_{o1} - \frac{v_{id}}{R_3}(R_2+R_3)$$

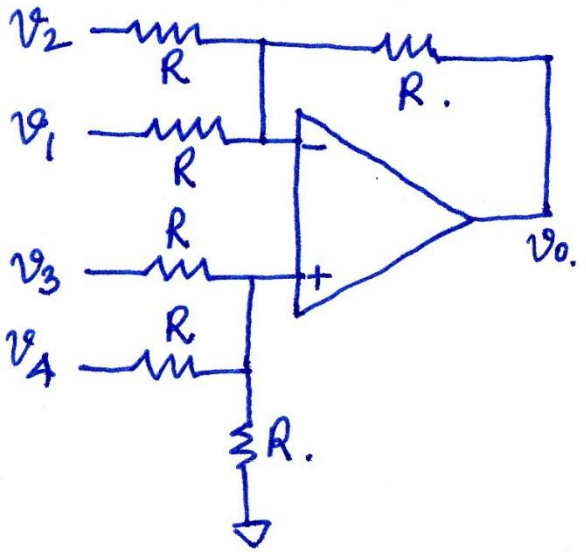
$$\text{or, } (v_{o1} - v_{o2}) = v_{id}\left(1+\frac{R_2}{R_3}\right)$$

Therefore, $$A_d = \frac{v_o}{v_{id}} = \frac{v_{o1}-v_{o2}}{v_{id}} \times \frac{v_o}{v_{o1}-v_{o2}} = \left(1+\frac{R_2}{R_3}\right)\left(\frac{R_f}{R_1}\right)$$

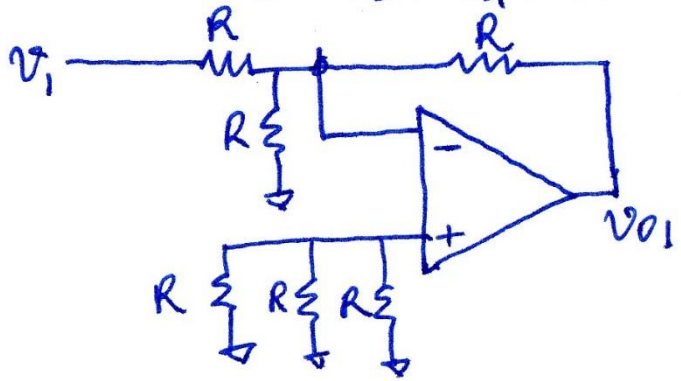
Adder/Subtractor :-

How to perform $(v_3+v_4)-(v_1+v_2)$?

use superposition theorem to analyse this ckt.



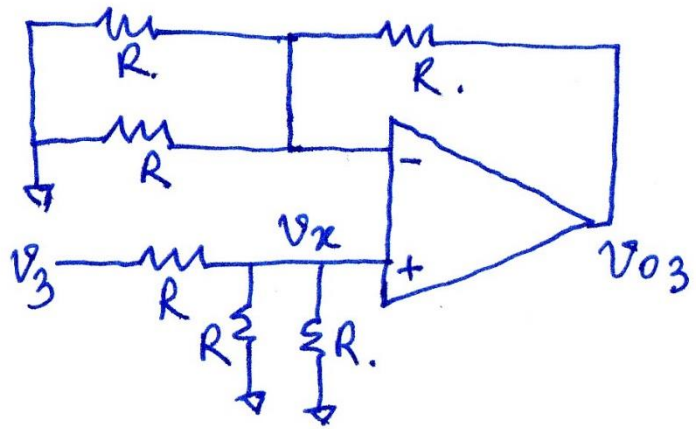
* Assume $v_2 = v_3 = v_4 = 0$.



$$v_{o1} = -\frac{R}{R} = -v_1$$

* Similarly, $v_{o2} = -v_2$ assuming $v_1 = v_3 = v_4 = 0$

* Assume $v_1 = v_2 = v_4 = 0$.



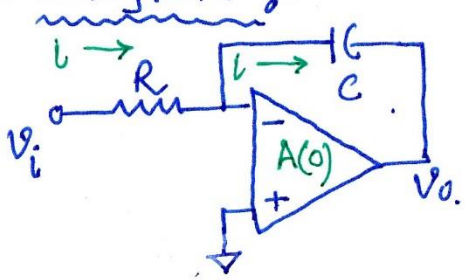
$$v_x = \frac{R/2}{R+R/2} v_3 = \frac{1}{3} v_3$$

$$v_{o3} = \left(1 + \frac{2R}{R}\right) v_x = 3 \times \frac{1}{3} v_3 = v_3.$$

* Similarly, $v_{o4} = v_4$ assuming $v_1 = v_2 = v_3 = 0$.

Therefore, $v_o = v_{o1} + v_{o2} + v_{o3} + v_{o4} = (v_3 + v_4) - (v_1 + v_2)$

Integrator :-



Time domain response :

$$\frac{v_i}{R} = i = -C\frac{dv_o}{dt}$$

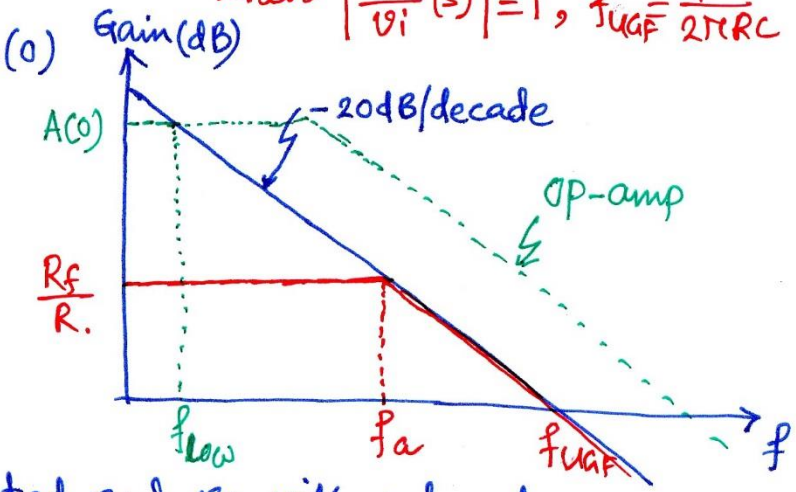
$$dv_o = -\frac{v_i}{RC}dt$$

$$v_o(t) = -\frac{1}{RC}\int_0^t v_i(t)\,dt + v_o(0)$$

Frequency domain response :-

$$\frac{v_o}{v_i}(s) = -\frac{1}{sRC}$$

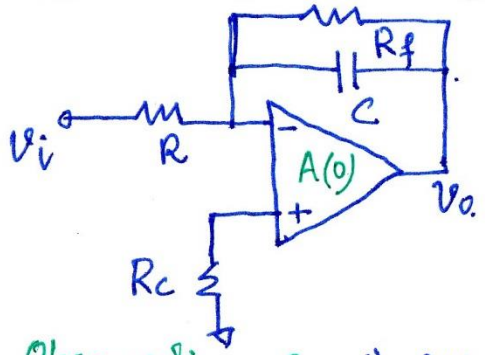
when $\left|\frac{v_o}{v_i}(s)\right| = 1$, $f_{UGF} = \frac{1}{2\pi RC}$



Problems :- 1) Op-amp limited dc gain alters frequency response at low frequency.
$f < f_{low}$ → it does not act as integrator.

2) Any dc offset will be integrated and v_o will saturate.

Improved configuration :-



$$\frac{v_o}{v_i}(s) = -\frac{R_f}{R}\cdot\frac{1}{(1+sR_fC)}$$

$$\left|\frac{v_o}{v_i}(0)\right| = +\frac{R_f}{R} \quad \text{and} \quad f_a = \frac{1}{2\pi R_f C}.$$

Observations :- 1) Below f_a, it does not act as an integrator.
2) Above f_a, integration starts with an accuracy of 50%.
3) Above $10f_a$, integration gives 99% accuracy.

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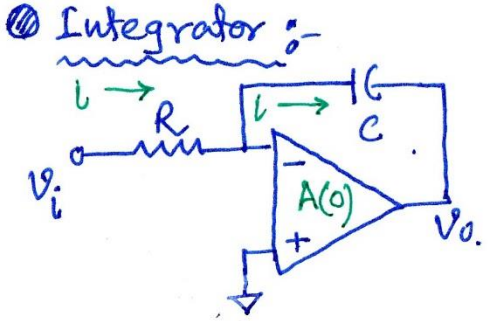
Integrator :-



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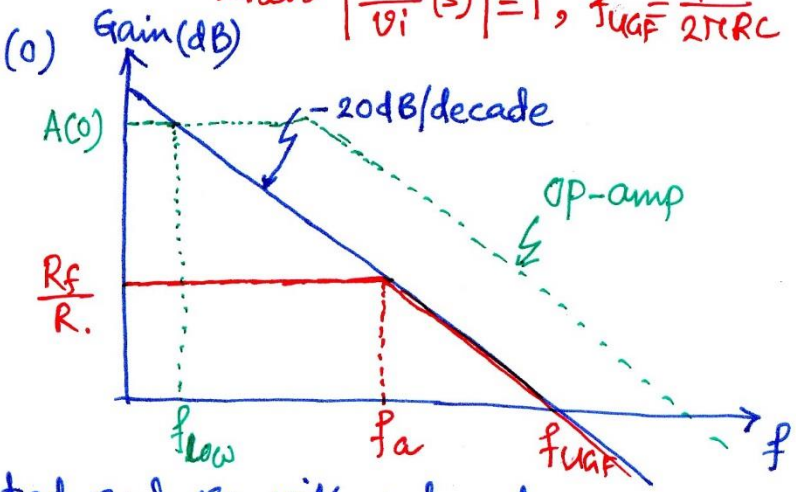

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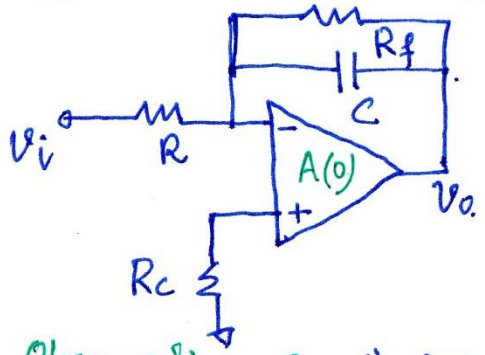

$$\frac{v_o}{v_i}(s) = -\frac{R_f}{R}\cdot\frac{1}{(1+sR_fC)}$$

$$\left|\frac{v_o}{v_i}(0)\right| = +\frac{R_f}{R} \quad \text{and} \quad f_a = \frac{1}{2\pi R_f C}.$$

Observations :- 1) Below f_a, it does not act as an integrator.
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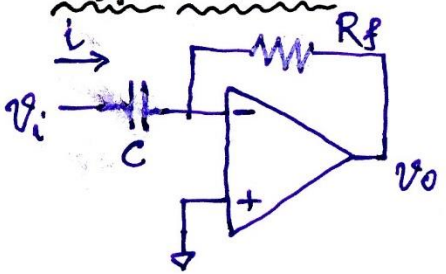
Differentiator :-



Time domain response

$i = C\frac{dv_i}{dt}$ where $i = \frac{-v_o}{R_f}$

$v_o = -iR_f$

$= -R_fC\frac{dv_i}{dt}$.

Frequency domain response

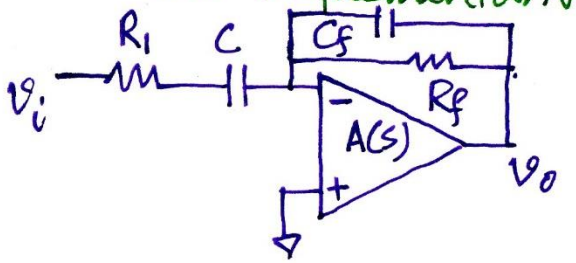
$\frac{v_o}{v_i}(s) = -\frac{R_f}{1/sC} = -sCR_f$.

$\left|\frac{v_o}{v_i}(s)\right| = sCR_f$

when $f_{UGF} = \frac{1}{2\pi CR_f}$, $\left|\frac{v_o}{v_i}\right| = 1$

Issue : High frequency noise is amplified.

Practical implementation :-



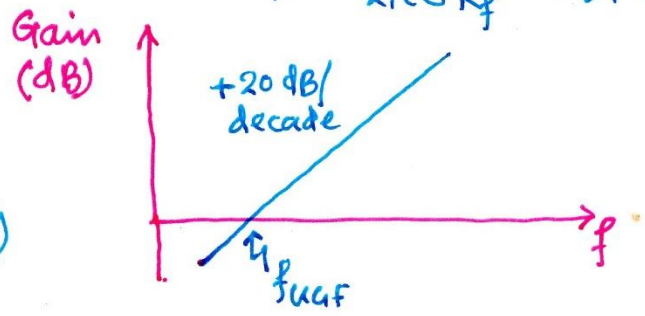
$\frac{v_o}{v_i}(s) = -\frac{sR_fC}{(1+sC_fR_f)(1+sCR_1)}$

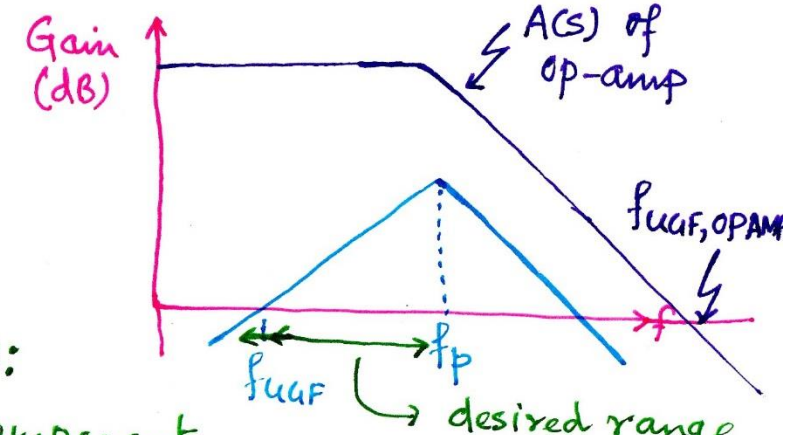
If $CR_1 = C_fR_f$

$\frac{v_o}{v_i}(s) = -\frac{sCR_f}{(1+sCR_1)^2}$

when $f_{UGF} = \frac{1}{2\pi R_fC}$, $\left|\frac{v_o}{v_i}\right| = 1$

$f_{p_1,2} = \frac{1}{2\pi CR_1}$





A good differentiator may be designed as follows:

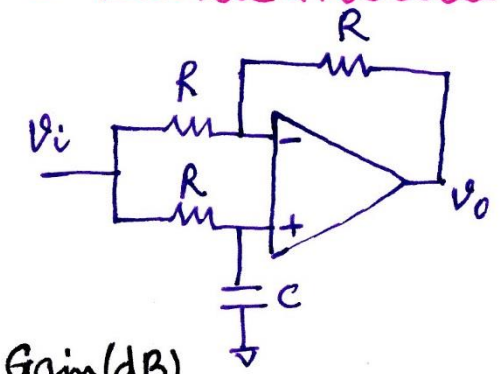
1) Fix $f_p = 10 f_{in}$ where f_{in} is highest freq. component of the input signal

2) Choose $f_{UGF,OPAMP} > f_p$

Phase Shift Circuits : (Also known as constant delay filter or all pass filter)

1) Constant DC gain 2) phase changes with frequency.

(*) Phase-lag circuit :-



inverting gain = −1 and non-inverting gain = $(1+\frac{R}{R}) = 2$.

Using voltage superposition :-

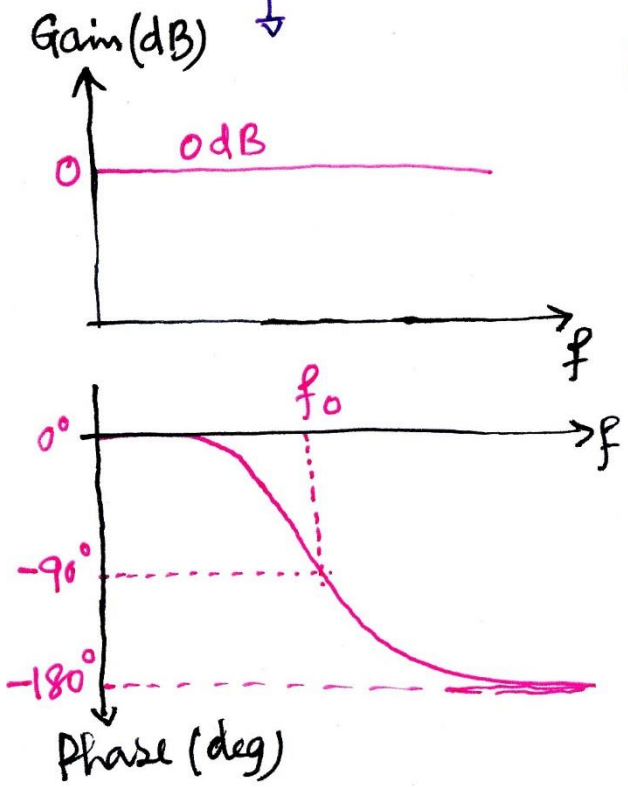
$$v_o(s) = -v_i(s) + 2v_i(s)/(1+sRC)$$

$$\boxed{\frac{v_o(j\omega)}{v_i(j\omega)} = \frac{1-j\omega RC}{1+j\omega RC}} \qquad \left|\frac{v_o}{v_i}\right| = 1.$$

Phase $\theta = -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC) = -2\tan^{-1}(\omega RC)$

$\omega \to 0$, $\theta = 0^\circ$ and $\omega \to \infty$, $\theta = -180^\circ$

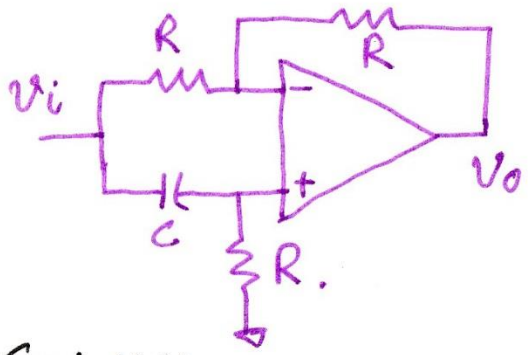
$\theta = -2\tan^{-1}\left(\frac{f}{f_0}\right)$ where $f_0 = \frac{1}{2\pi RC}$



Try yourself :-

Determine the phase angle and the time delay for the circuit shown in figure for a frequency of 2 kHz. $R = 39\,k\Omega$, $C = 1\,nF$.

✱ Phase lead circuit :-



Using voltage superposition :-

$$v_o(s) = -v_i(s) + 2v_i(s)\cdot\frac{R}{R+\frac{1}{sC}} = -v_i(s) + \frac{2sRC}{1+sRC}v_i(s)$$

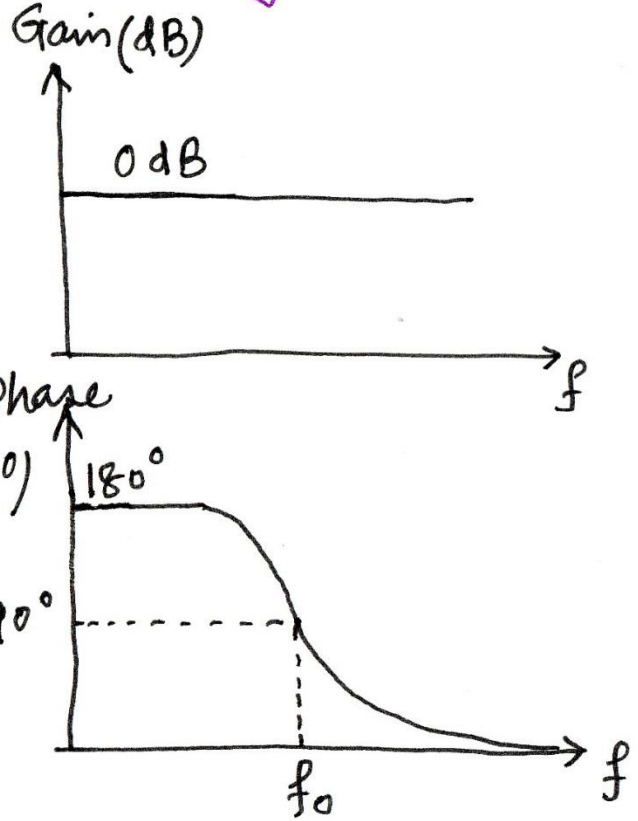
$$v_o(j\omega) = -v_i(j\omega) + \frac{2j\omega RC}{1+j\omega RC}v_i(j\omega)$$

$$\boxed{\frac{v_o(j\omega)}{v_i(j\omega)} = -\frac{1-j\omega RC}{1+j\omega RC}} \qquad \left|\frac{v_o}{v_i}\right| = 1.$$

Phase $\theta = 180^\circ - \tan^{-1}(\omega RC) - \tan^{-1}(\omega RC) = 180^\circ - 2\tan^{-1}(\omega RC)$

$\omega \to 0$, $\theta \to 180^\circ$ and $\omega \to \infty$, $\theta = 0^\circ$.

$\theta = 180^\circ - 2\tan^{-1}(f/f_0)$. where $f_0 = \frac{1}{2\pi RC}$.



Try yourself :-

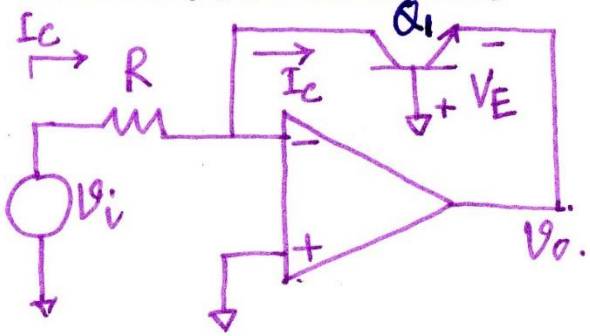
Determine the phase angle and the time delay for the circuit shown in figure for a frequency of 2KHz.

where $R = 39\,k\Omega$, $C = 1\,nF$.

Logarithmic Amplifier :-

Applications : To compress large dynamic range. Used in spectrum analyzer, multiplier etc.

* Basic structure :-



$$I_E = I_S\left[e^{\frac{qV_E}{KT}} - 1\right]$$

$$I_C \approx I_S\left[e^{\frac{qV_E}{KT}} - 1\right]$$

$$\frac{I_C}{I_S} = e^{qV_E/KT} - 1$$

Where I_S = emitter saturation current $\approx 10^{-13}$ A

K = Boltzman Constant

T = Absolute temperature

$$\Rightarrow e^{qV_E/KT} = \frac{I_C}{I_S} + 1 \approx \frac{I_C}{I_S} \quad \text{as } I_C >> I_S$$

$$\text{or, } \ln e^{qV_E/KT} = \ln\left[\frac{I_C}{I_S}\right]$$

$$\text{or, } V_E = \frac{KT}{q}\ln\left[\frac{I_C}{I_S}\right] = \frac{KT}{q}\ln\left[\frac{v_i}{RI_S}\right]$$

$$\text{or, } v_E = \frac{KT}{q}\ln\left[\frac{v_i}{v_{Ref}}\right] \quad \text{where } v_{Ref} = I_S R.$$

Now, $V_E = -V_o$

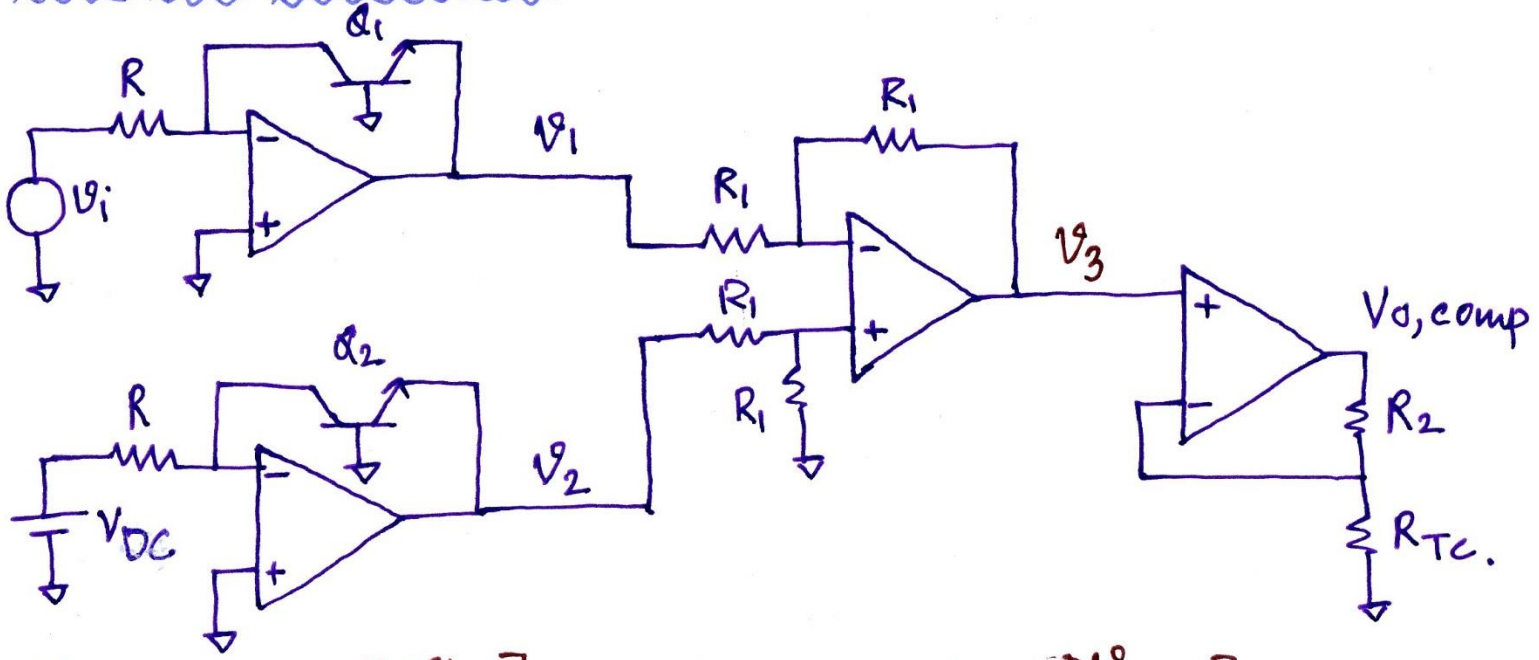
$$\text{or, } V_o = -\frac{KT}{q}\ln\left[\frac{v_i}{v_{Ref}}\right].$$

$$\text{or, } v_o = -\frac{KT}{q}\log_{10}\left[\frac{v_i}{v_{Ref}}\right]\cdot\frac{1}{0.4343}$$

Problem : 1) I_S varries from transistor to transistor.

2) V_o still depends on temperature T.

* Modified structure :-



$$v_1 = -\frac{KT}{q} \ln\left[\frac{v_i}{I_S R}\right] \quad \text{and} \quad v_2 = -\frac{KT}{q} \ln\left[\frac{v_{DC}}{I_S R}\right]$$

$$-(v_1 - v_2) = v_3 = v_2 - v_1 = -\frac{KT}{q} \ln\left[\frac{v_{DC}}{I_S R}\right] + \frac{KT}{q} \ln\left[\frac{v_i}{I_S R}\right] = \frac{KT}{q} \ln\left[\frac{v_i}{v_{DC}}\right].$$

The variation of I_S has been eliminated in v_3. It is still dependent on T.

$$v_{o,comp} = \left(1 + \frac{R_2}{R_{TC}}\right) \frac{KT}{q} \ln\left[\frac{v_i}{v_{DC}}\right]$$

where R_{TC} is temperature-sensitive resistance with a positive co-efficient. R_{TC} is also known as sensistor.

- Requires four op-amps → expensive.

EE60032: Analog Signal Processing

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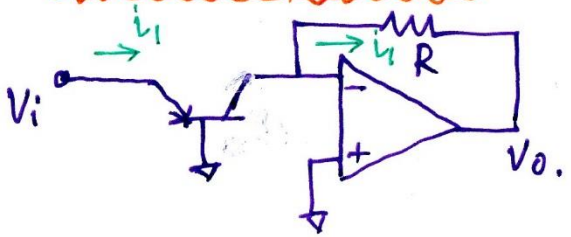
Antilogarithmic Amplifier :-

Logarithimically encoded signal will be decoded by this ckt.

- **Basic Antilog ckt :-**

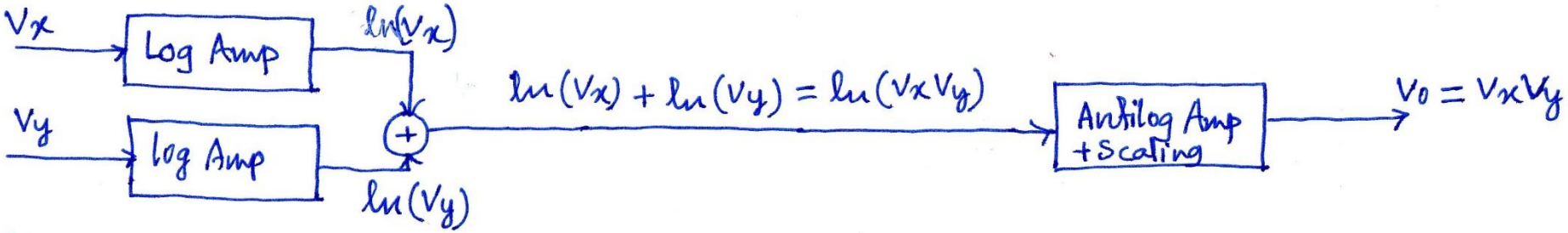


$$v_o = -i_1 R \quad \text{where} \quad I_E = I_1 \approx I_s e^{qv_i/kT}.$$

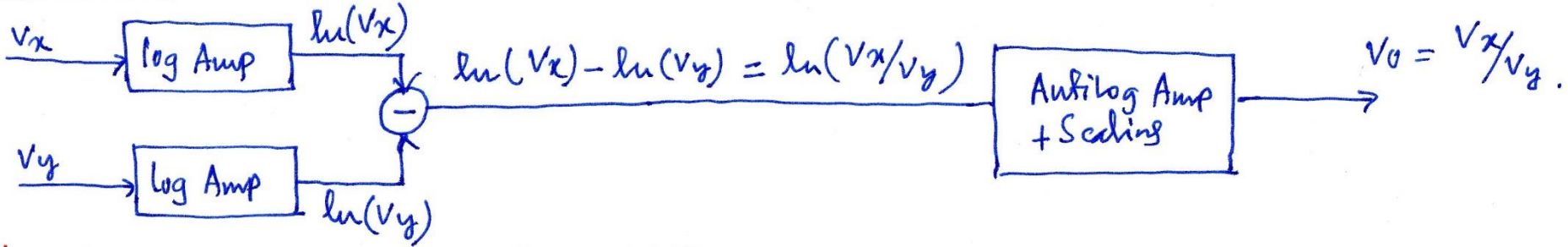
$$v_o = -I_s R e^{qv_i/kT}.$$

Applications of logarithimic and antilogarithimic amplifiers :-

- **Multiplication :-** V_x and V_y are two signals.



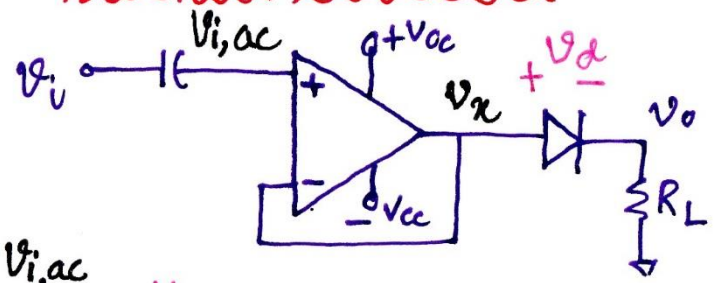
- **Division :-**

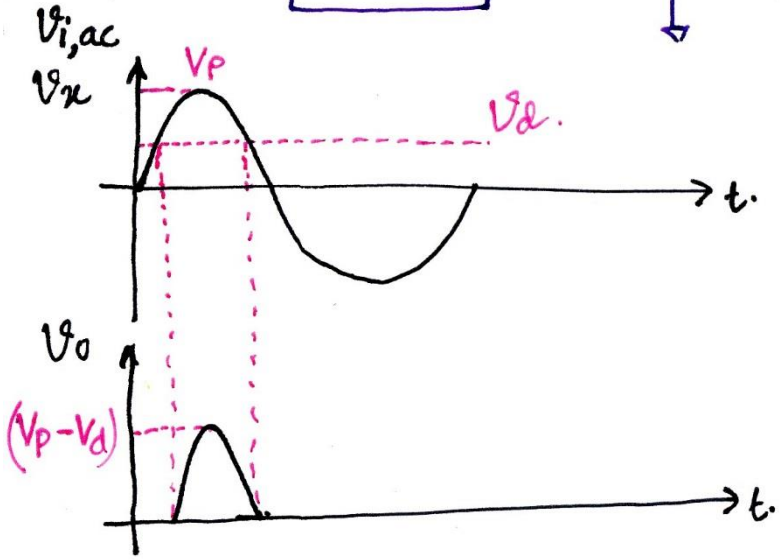


Limitation :- Single quadrant multiplier.

Rectifier Circuits :- To process AC signals

* Half-wave rectifier :-

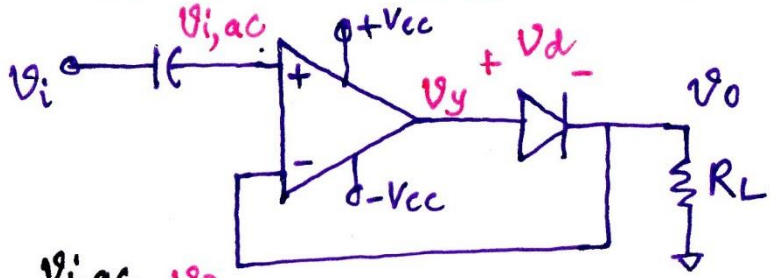




Limitations :- 1) v_o always has diode forward bias drop. $V_d \approx 700$ mV.

2) If $V_P < V_d$, the signal will be lost.

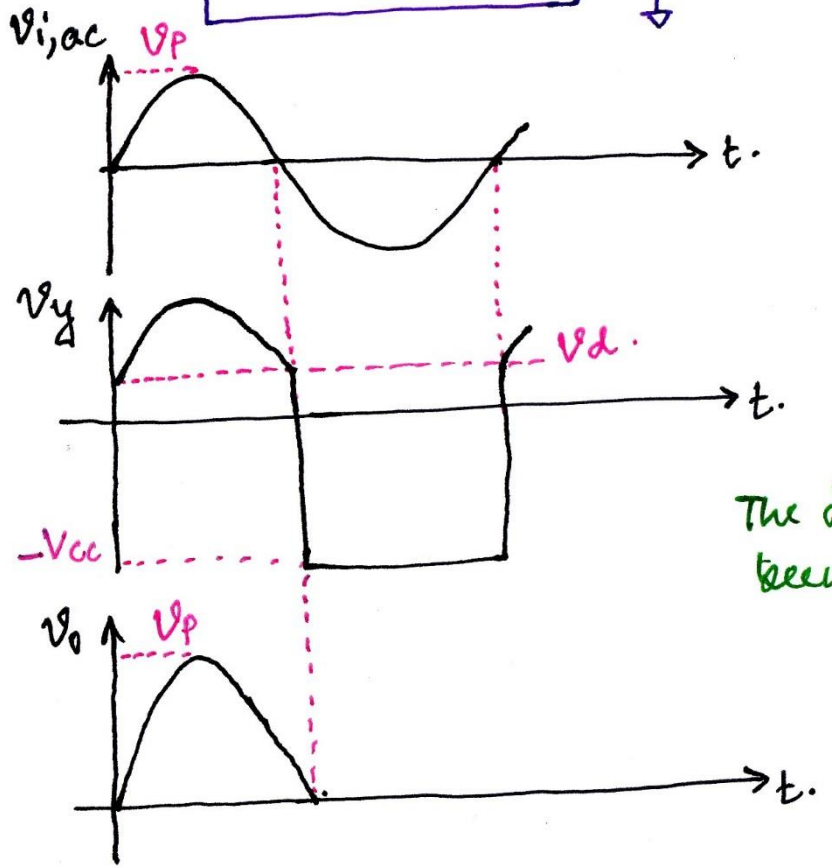
* Half-wave precesion rectifier :-



If $v_{i,ac} = 0 = v_o$, $v_y = V_d$

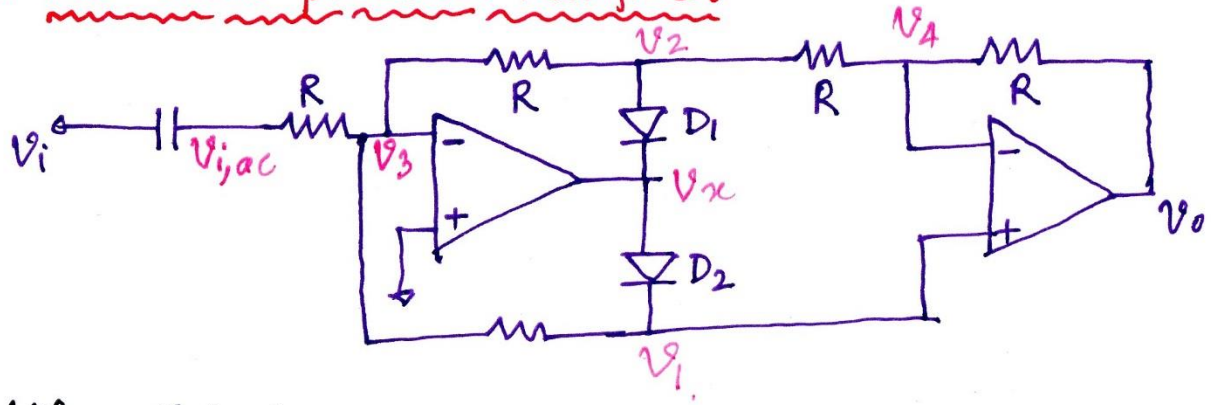
If $v_{i,ac} > 0$, $v_y \uparrow$, $v_o = v_{i,ac}$

If $v_{i,ac} < 0$, diode is off, $v_y = -V_{cc}$.



The diode drop has been eliminated.

* Full-wave precision rectifier:-



Operation:-

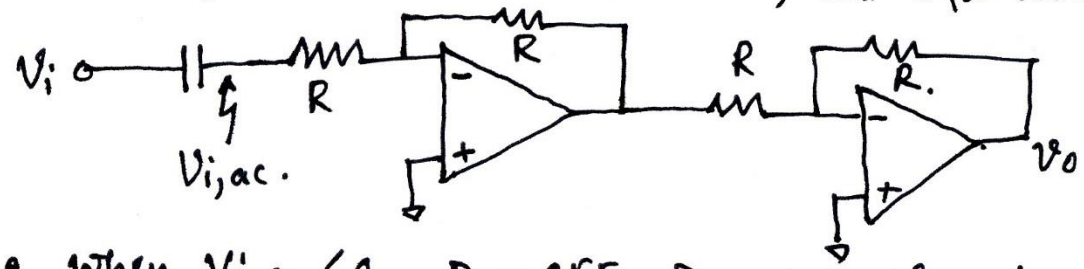
1) $v_{i,ac} = 0$, $v_3 = v_1 = v_4 = v_2 = 0$
$v_x = -0.7$ V, $D_1 = ON$. $D_2 = OFF$

2) $v_{i,ac} > 0$, $D_1 = ON$, $D_2 = OFF$.

3) $v_{i,ac} < 0$, $D_2 = ON$, $D_1 = OFF$.

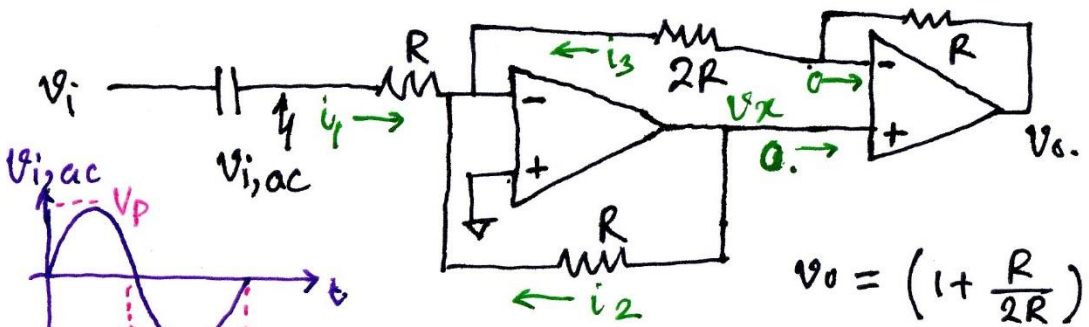
No diode drop appears at the o/p v_o. Diodes are placed inside the loop.

- When $v_{i,ac} > 0$, $D_1 = ON$, $D_2 = OFF$., then equivalent ckt.



$v_o = v_{i,ac}$.

- when $v_{i,ac} < 0$, $D_1 = OFF$, $D_2 = ON$. then the equivalent circuit is given below.



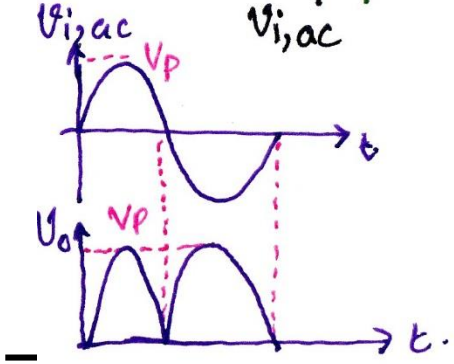
$$i_1 + i_2 + i_3 = 0.$$

$$\frac{v_{i,ac}}{R} + \frac{v_x}{2R} + \frac{v_x}{R} = 0.$$

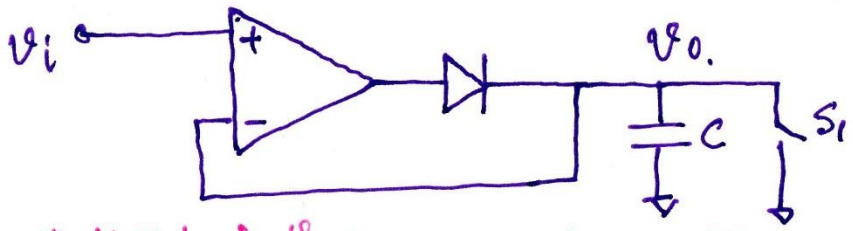
$$\text{or, } v_x = -\frac{2}{3} v_{i,ac}.$$

$$v_o = \left(1 + \frac{R}{2R}\right) v_x$$

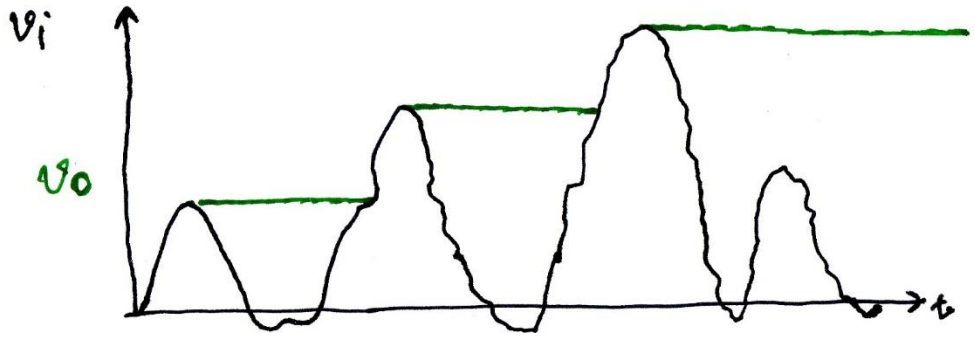
$$= -\frac{3}{2} \times \frac{2}{3} v_{i,ac} = -v_{iac}.$$



● Peak Detector Circuit :- To detect the maximum peak of a signal.

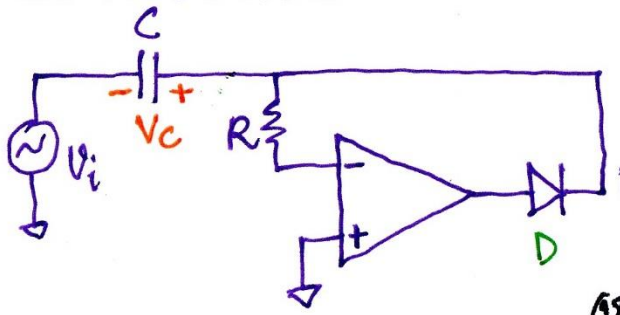


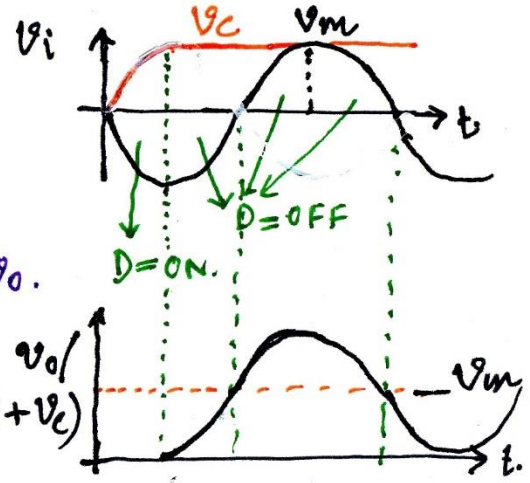
* w.r.t. half wave precision rectifier, here capacitor is used instead of resistor, at v_o.



● Voltage Clamper Circuit :- To insert a DC / Common mode level with a signal.

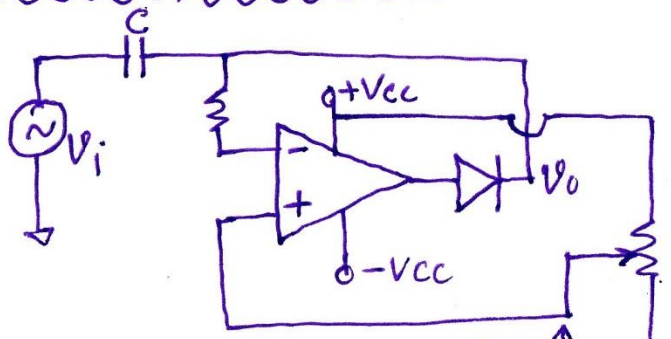
Basic concept :-

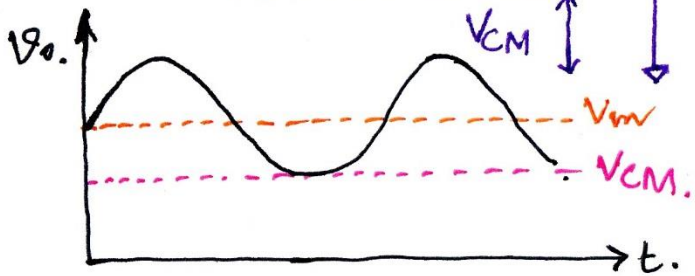




The capacitor stores the peak value of the signal and the diode becomes off permanently. The o/p v_o is dc shifted by V_m

Modified structure :-





EE60032: Analog Signal Processing

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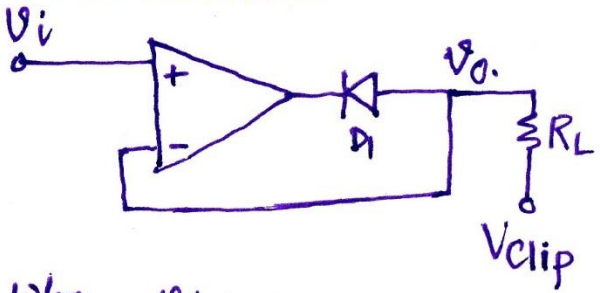
Clipper :- To cut-out/remove some portion of the signal above/below clipping voltage. A half-wave rectifier circuit can be treated as a clipper circuit clipping at 0V.

* **Positive clipper :-** When clipping is done above clipping voltage V_{clip}

Basic concept :-

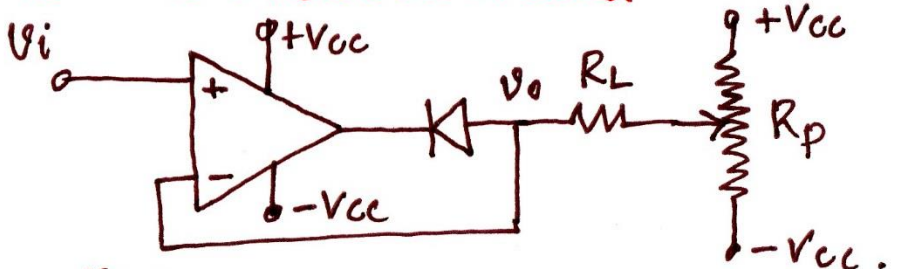


When $v_i \geq V_{clip}$, $D_1 = OFF$, $v_o = V_{clip}$.

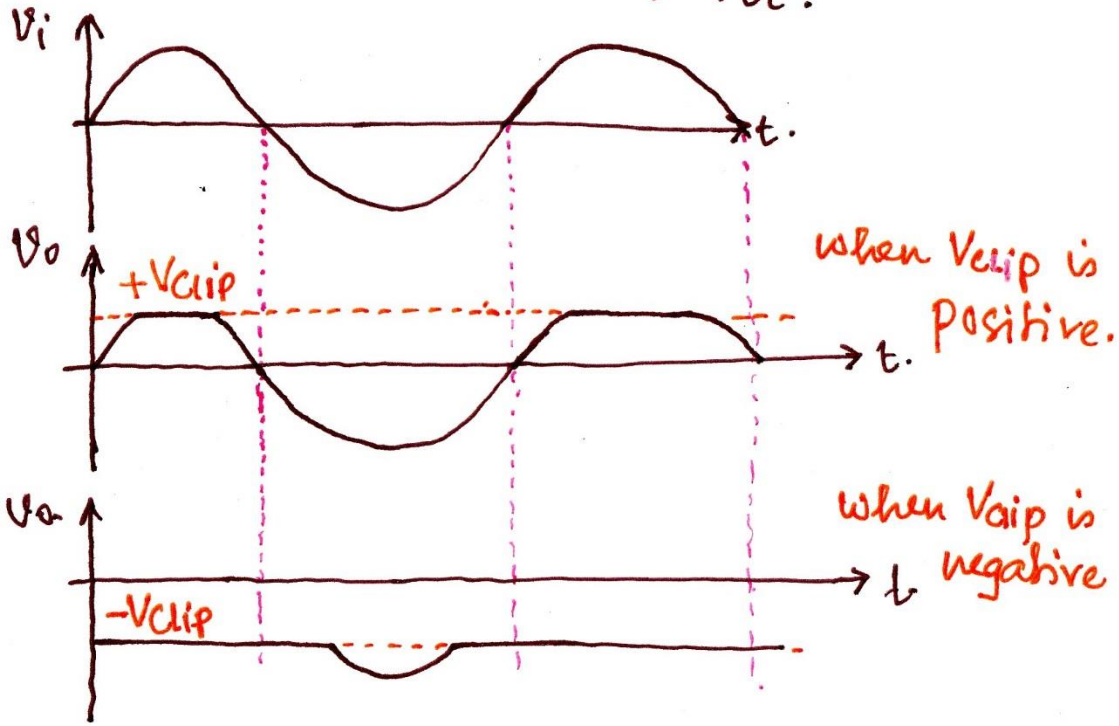
When $v_i < V_{clip}$, $D_1 = ON$, $v_o = v_i$

Depending on the position of the jockey in R_P, $+V_{clip}$ or $-V_{clip}$ voltage can be generated.

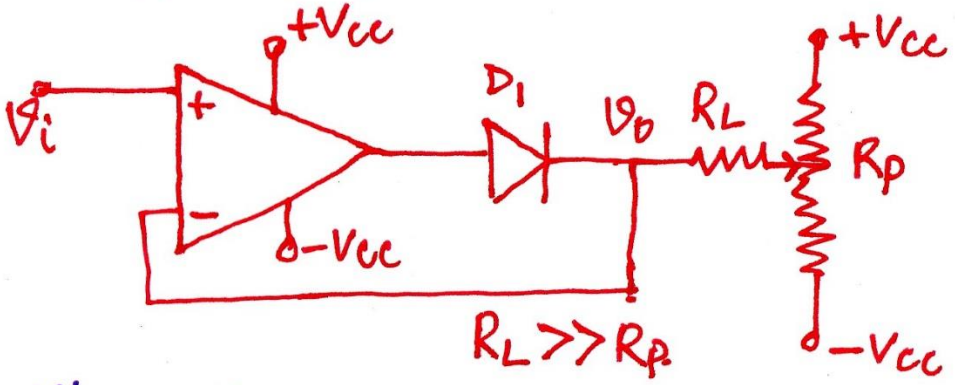
Practical Implementation :-



$R_L >> R_P$

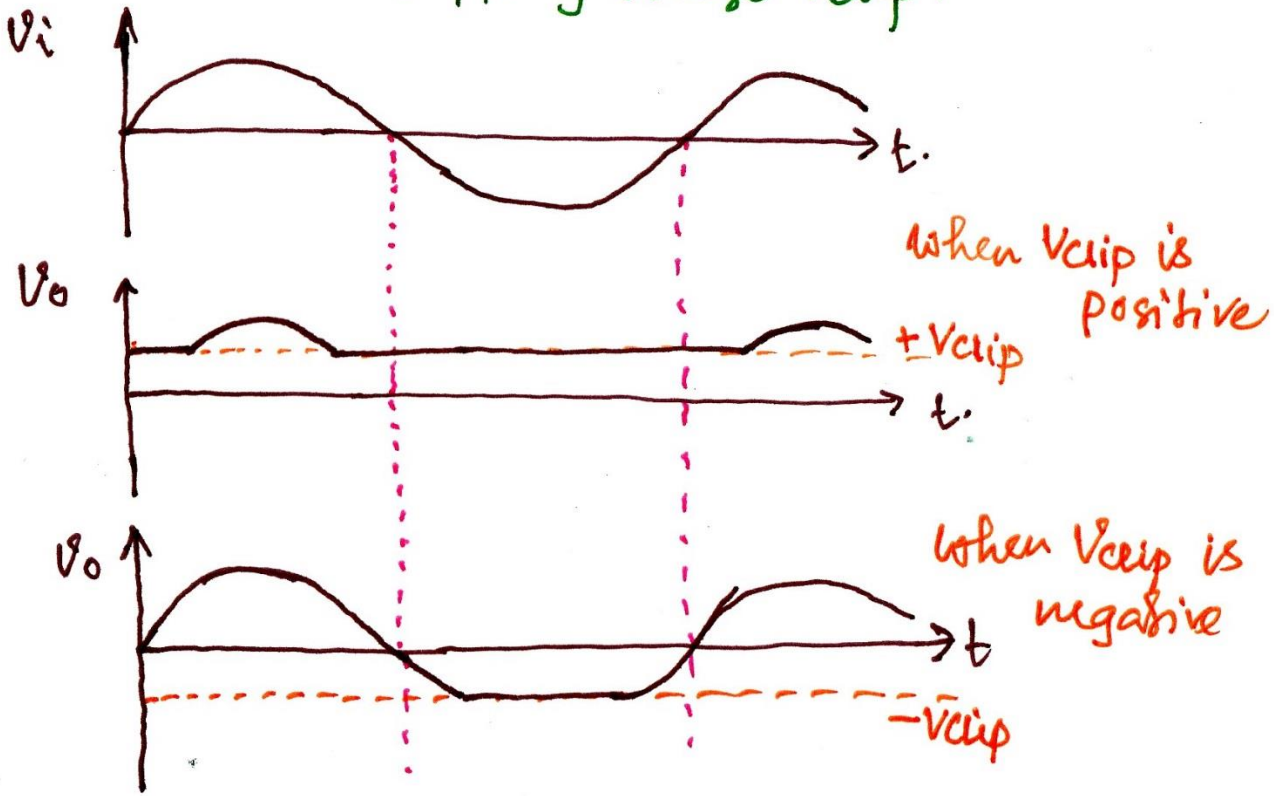


* Negative clipper :- When clipping is done below the clipping voltage V_{clip}.

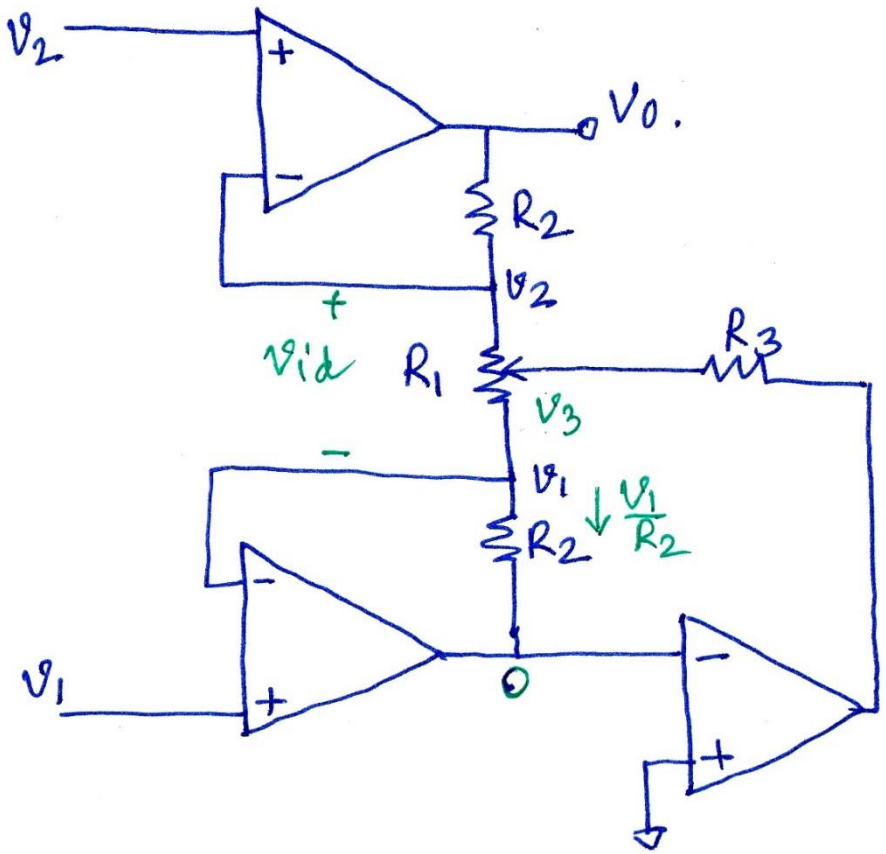


When $v_i > V_{clip}$, $D_1 = ON$, $v_o = v_i$

When $v_i \leq v_{clip}$, $D_1 = OFF$, $v_o = V_{clip}$



Tutorial problems :-



If the wiper positioned at the middle, show that :-

$$v_o = \left(1 + \frac{2R_2}{R_1}\right)(v_2 - v_1)$$

$$v_3 = \frac{v_1}{R_2}\cdot\left(R_2 + \frac{R_1}{2}\right) = v_1\left(1 + \frac{R_1}{2R_2}\right).$$

$$\frac{v_o - v_2}{R_2} = \frac{v_2 - v_3}{R_1/2}$$

$$\frac{v_o - v_2}{R_2} = \frac{2(v_2 - v_3)}{R_1}$$

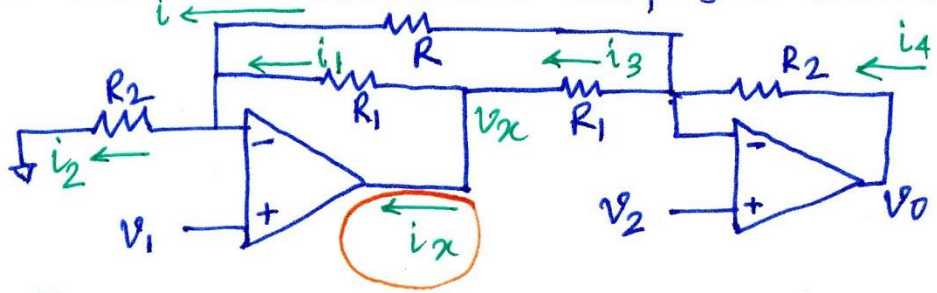
or, $R_1 v_o - R_1 v_2 = 2R_2 v_2 - 2R_2 v_3$

or, $R_1 v_o = v_2[2R_2 + R_1] - 2R_2 v_1\left[1 + \frac{R_1}{2R_2}\right]$.

or, $R_1 v_o = v_2[R_1 + 2R_2] - v_1[2R_2 + R_1]$.

or, $v_o = (v_2 - v_1)\left[1 + \frac{2R_2}{R_1}\right]$.

⊛ For the instrumentation amplifier shown in figure, verify $v_o = \left(1 + \frac{R_2}{R_1} + \frac{2R_2}{R}\right)(v_2 - v_1)$

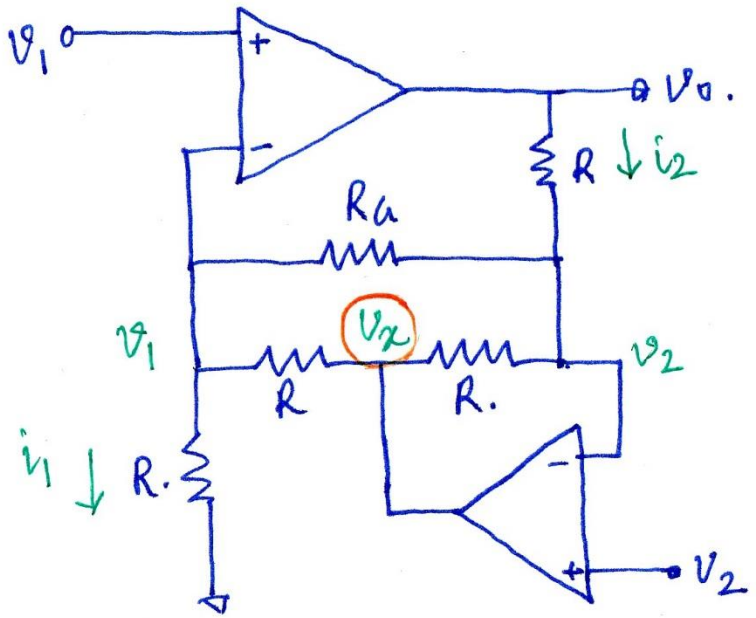


$$i_2 = \frac{v_1}{R_2}, \quad i_4 = \frac{v_o - v_2}{R_2}, \quad i = \frac{v_2 - v_1}{R}$$

$$i_1 = \frac{v_x - v_1}{R_1}, \quad i_3 = \frac{v_2 - v_x}{R_1}$$

Rest you try yourself to solve.

⊛ For the given amplifier below, show that $v_o = 2\left(1 + \frac{R}{R_G}\right)(v_2 - v_1)$



$$i_1 = \frac{v_1}{R}, \quad i_2 = \frac{v_o - v_2}{R}$$

$$i_1 = \frac{v_x - v_1}{R} + \frac{v_2 - v_1}{R_G}$$

$$i_2 = \frac{v_2 - v_1}{R_G} + \frac{v_2 - v_x}{R}$$

Rest you try yourself to solve.